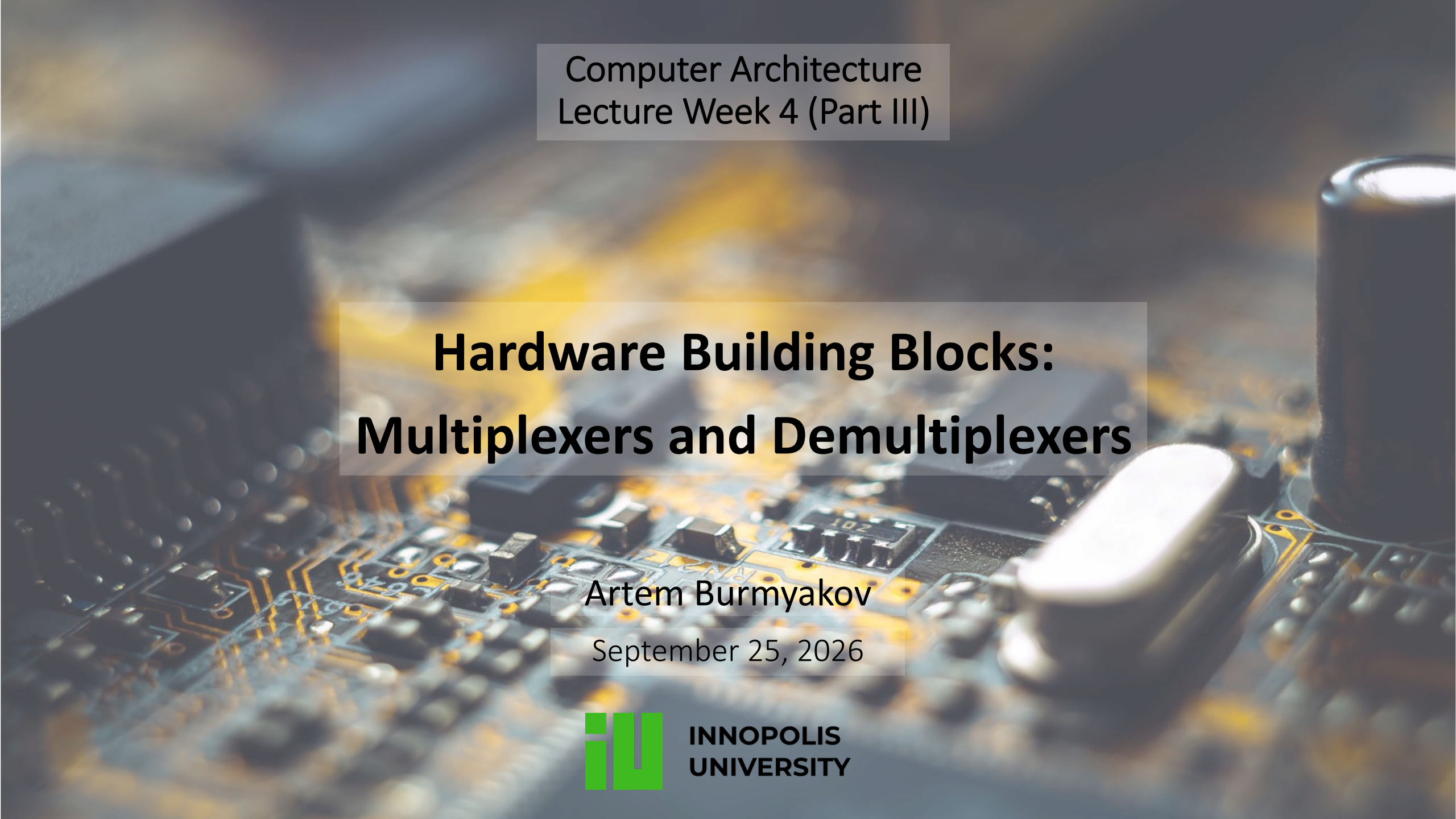




Computer Architecture
Lecture Week 4 (Part III)

Hardware Building Blocks: Multiplexers and Demultiplexers

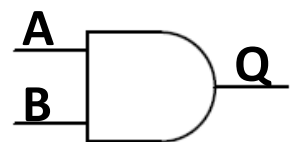
Artem Burmyakov

September 25, 2026



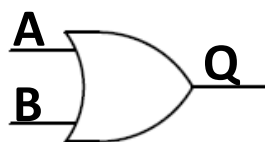
INNOPOLIS
UNIVERSITY

Recap: Basic Logic Gates



AND

A	B	Output
0	0	0
0	1	0
1	0	0
1	1	1



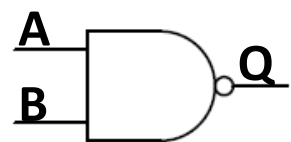
OR

A	B	Output
0	0	0
0	1	1
1	0	1
1	1	1



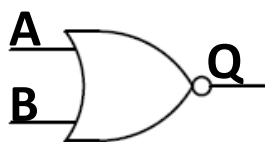
XOR

A	B	Output
0	0	0
0	1	1
1	0	1
1	1	0



NAND

A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0



NOR

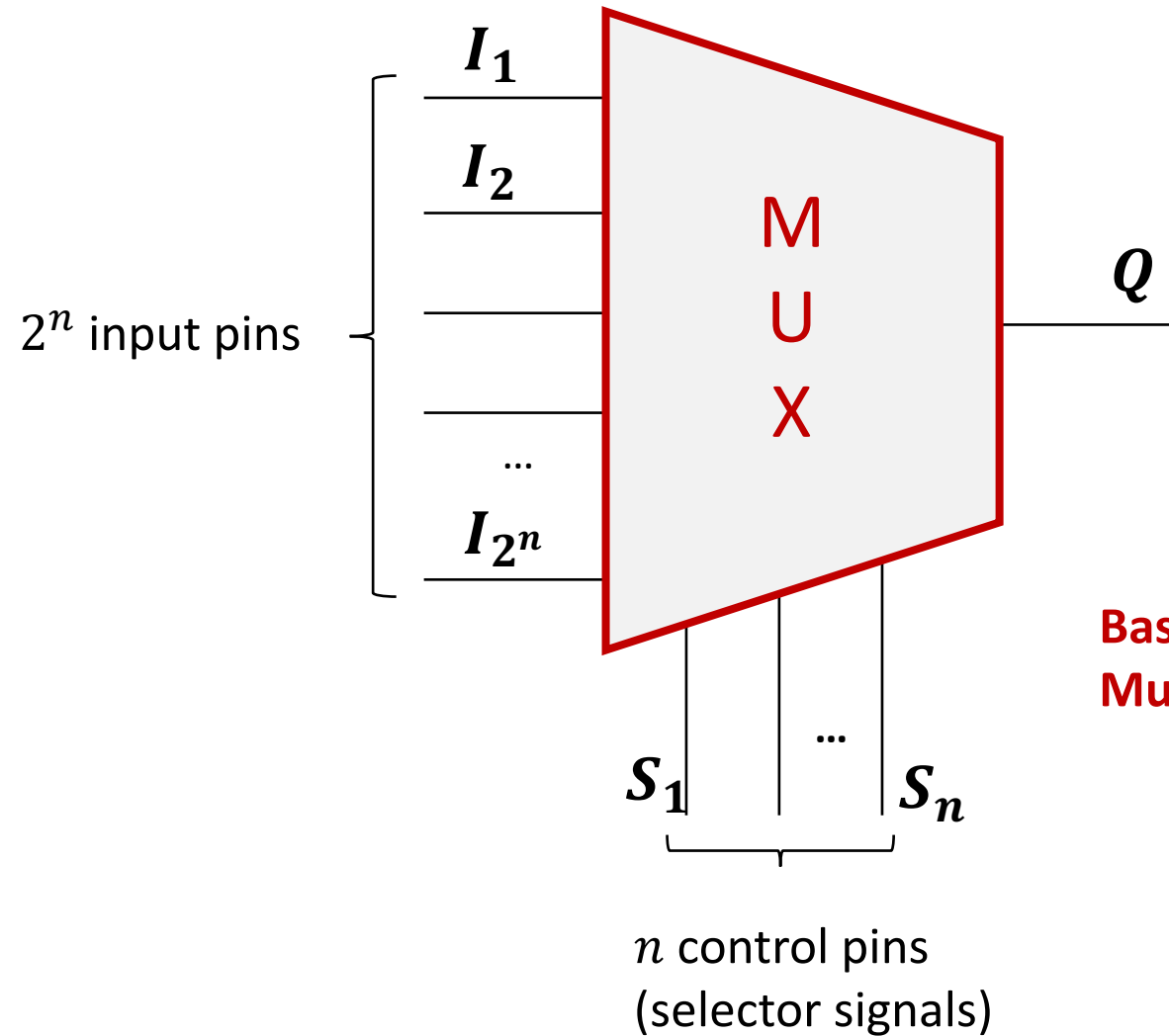
A	B	Output
0	0	1
0	1	0
1	0	0
1	1	0



XNOR

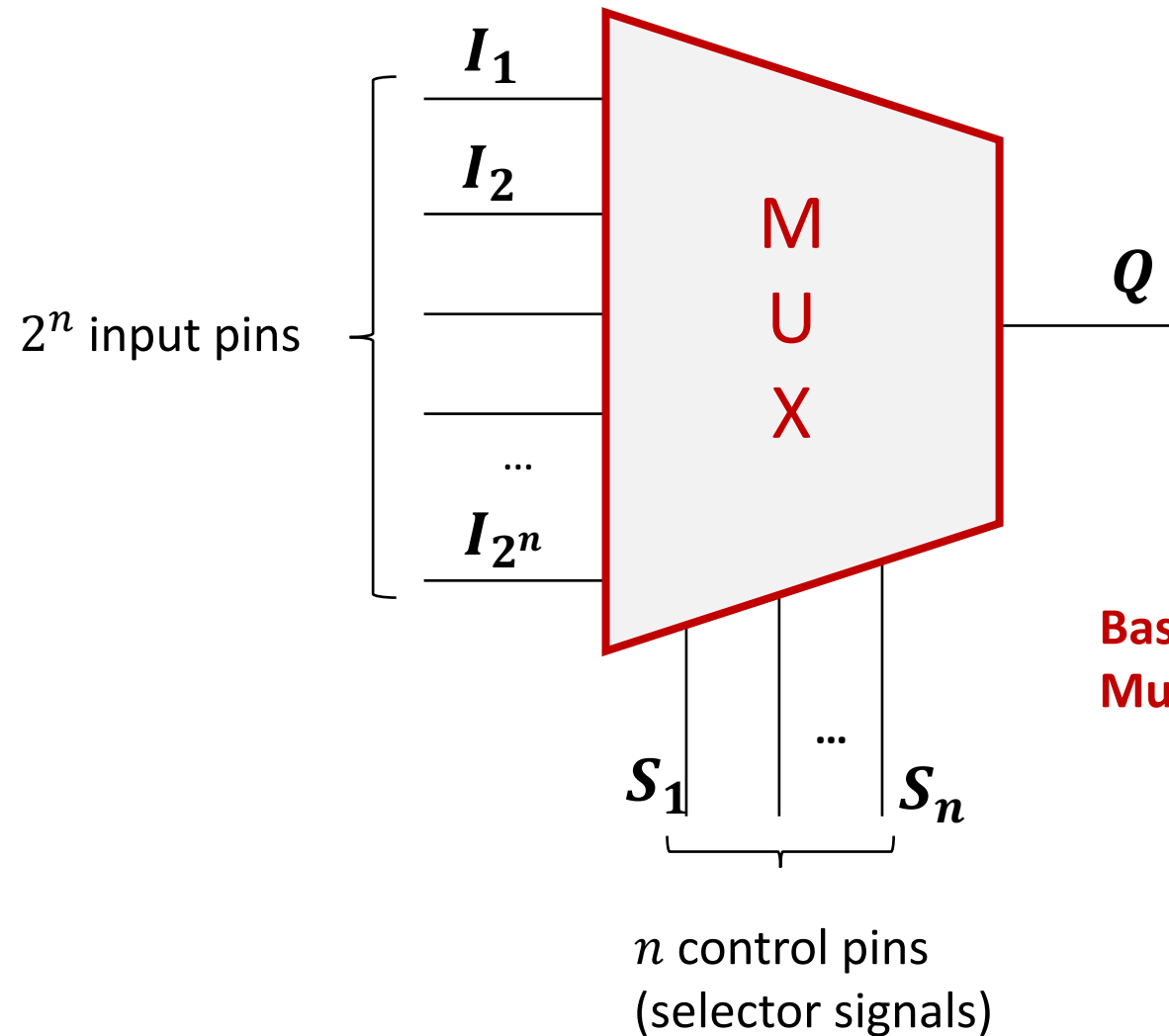
A	B	Output
0	0	1
0	1	0
1	0	0
1	1	1

Consider the following circuit:



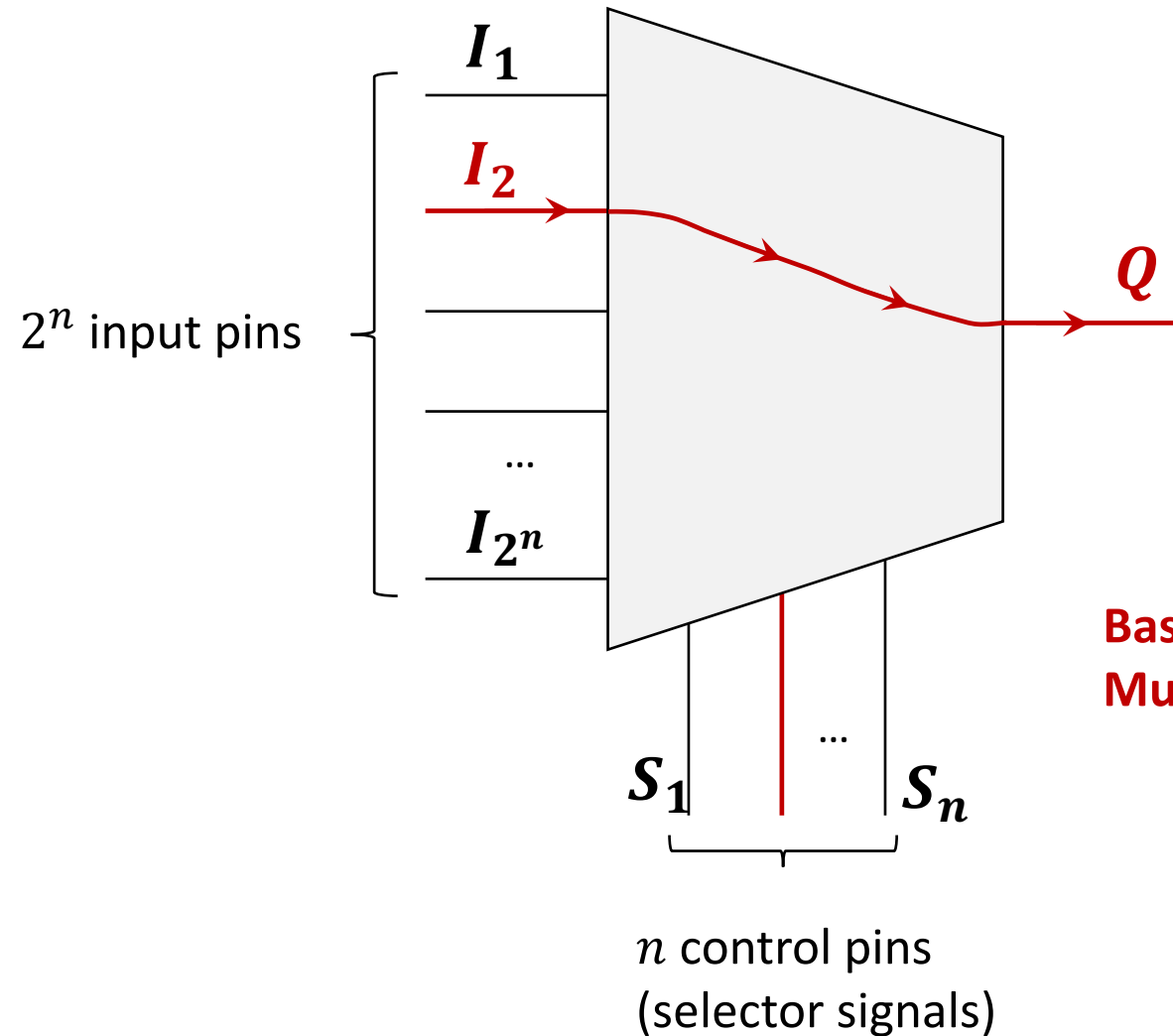
**Based on control pin signals,
Multiplexer sets its output to one of its inputs**

Multiplexer (or Selector): Combinational Logic Circuit



**Based on control pin signals,
Multiplexer sets its output to one of its inputs**

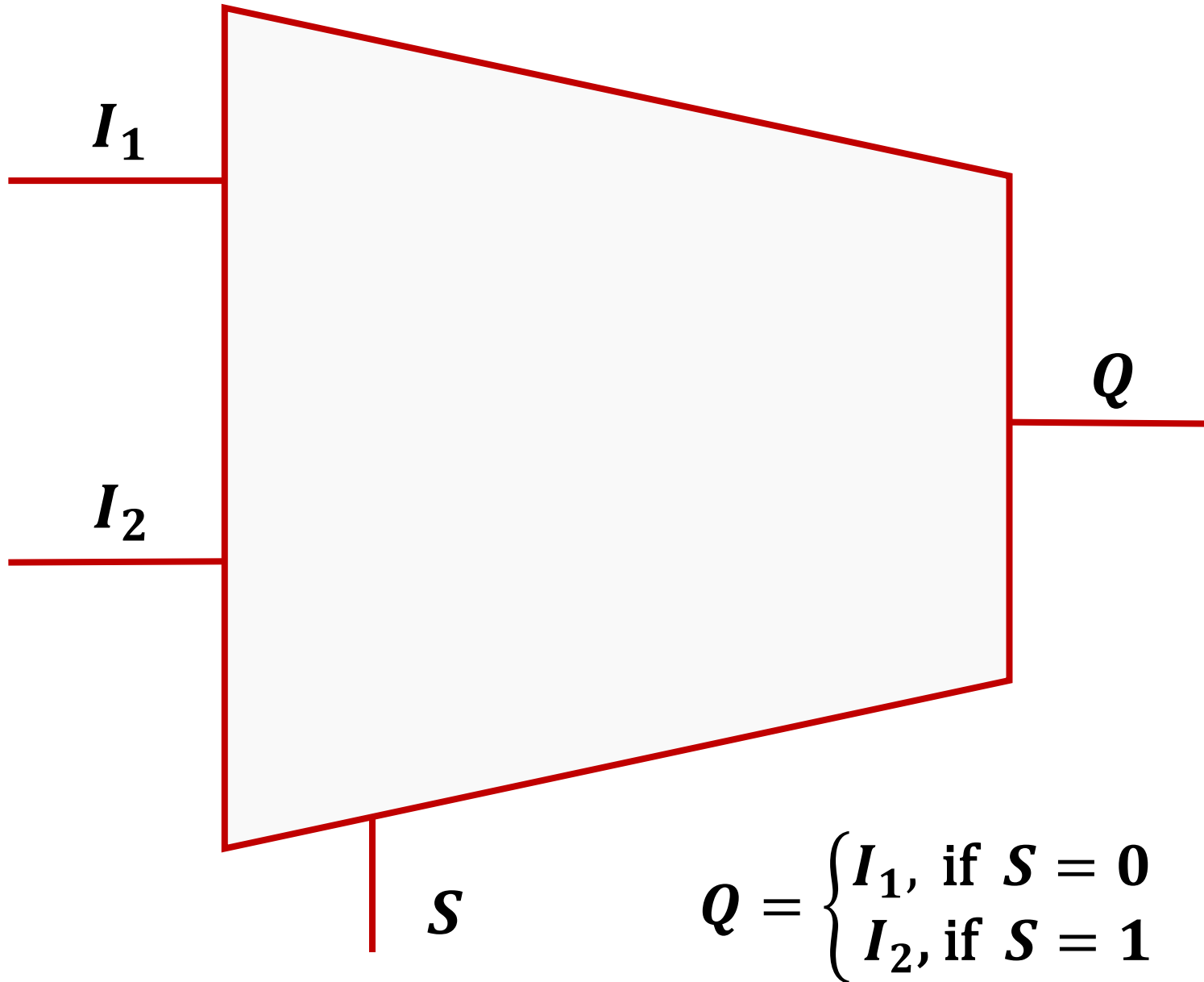
Multiplexer (or Selector): Combinational Logic Circuit



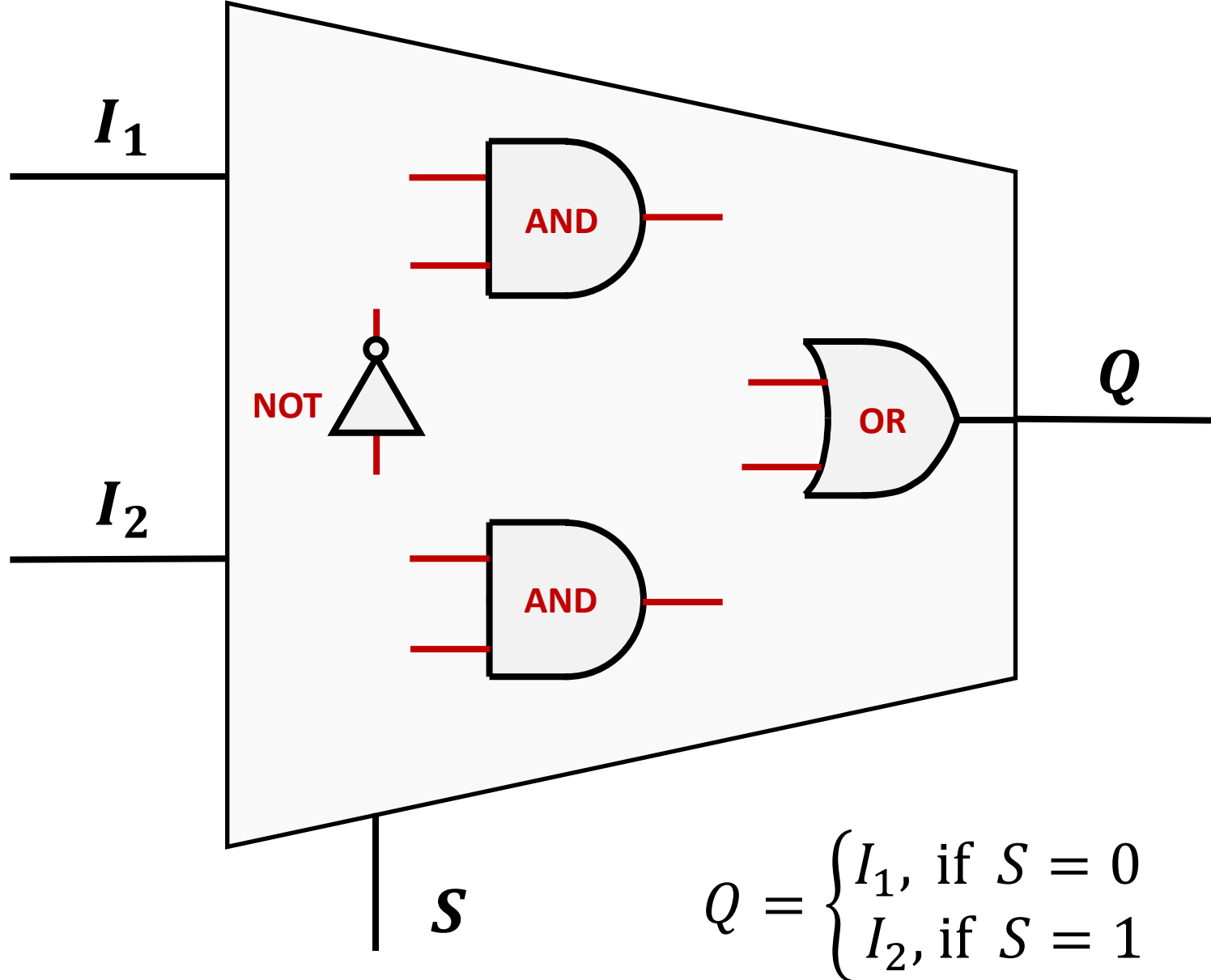
**Based on control pin signals,
Multiplexor sets its output to one of its inputs**

2-to-1 Multiplexer Implementation

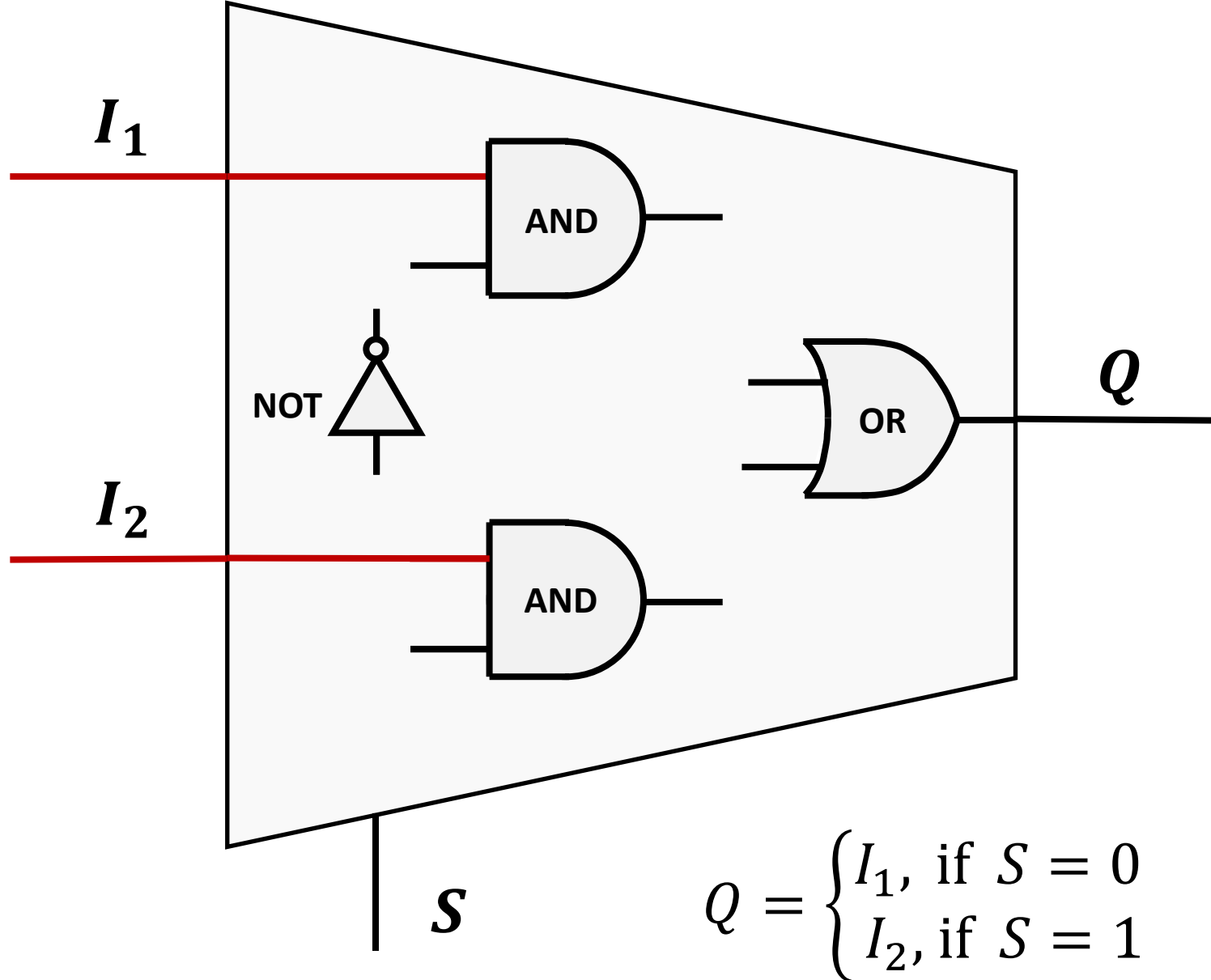
2-to-1 Multiplexer Implementation



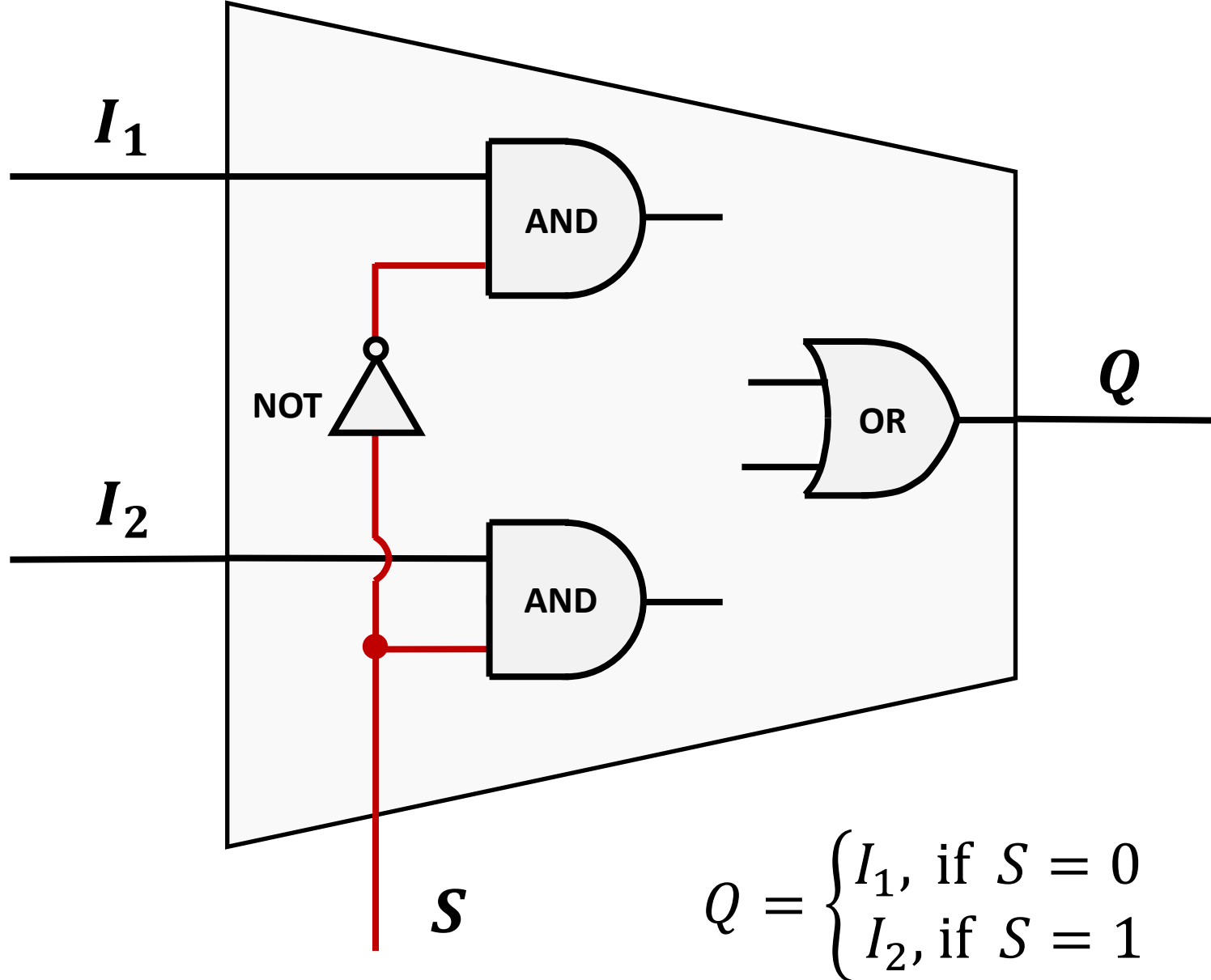
2-to-1 Multiplexer Implementation



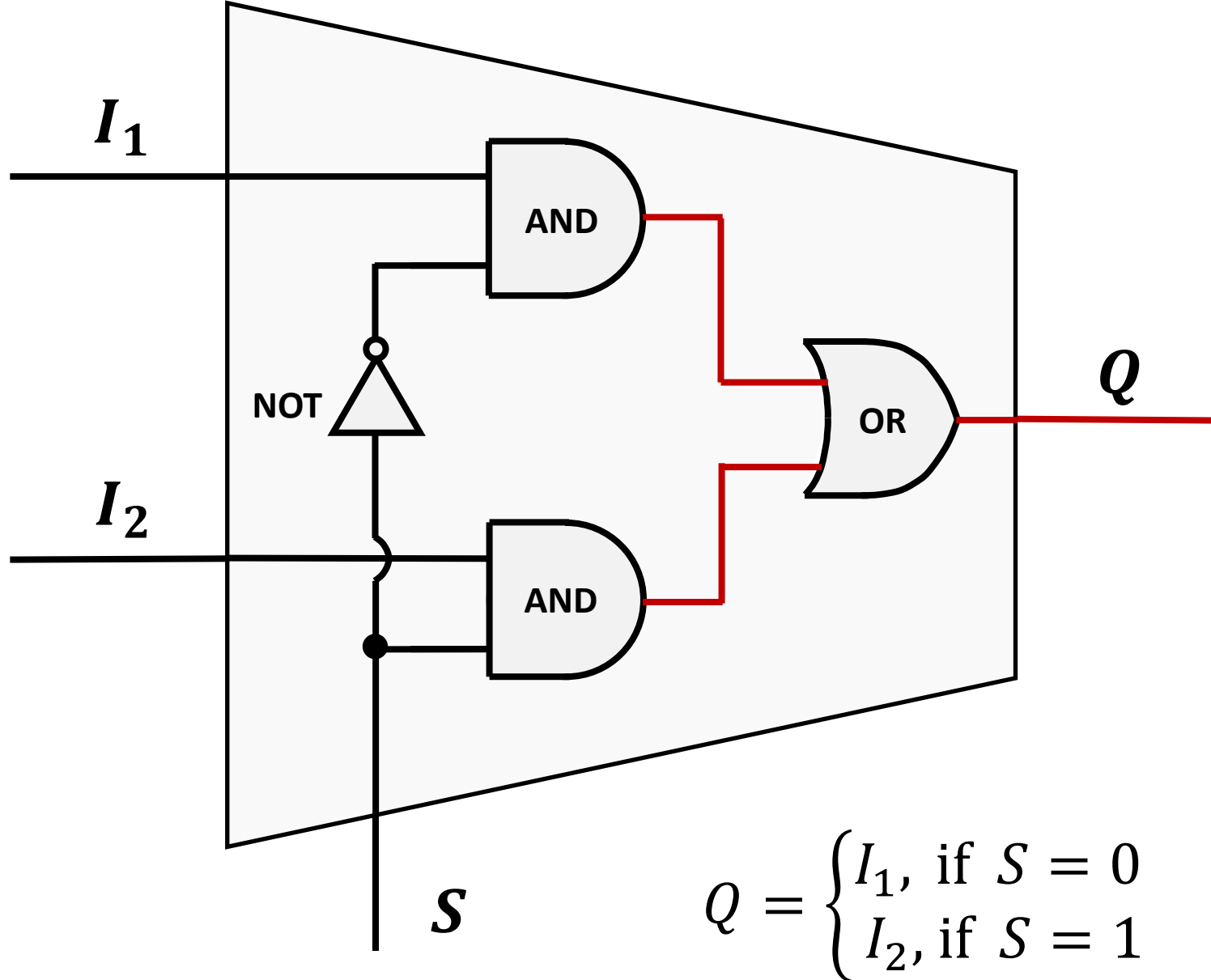
2-to-1 Multiplexer Implementation



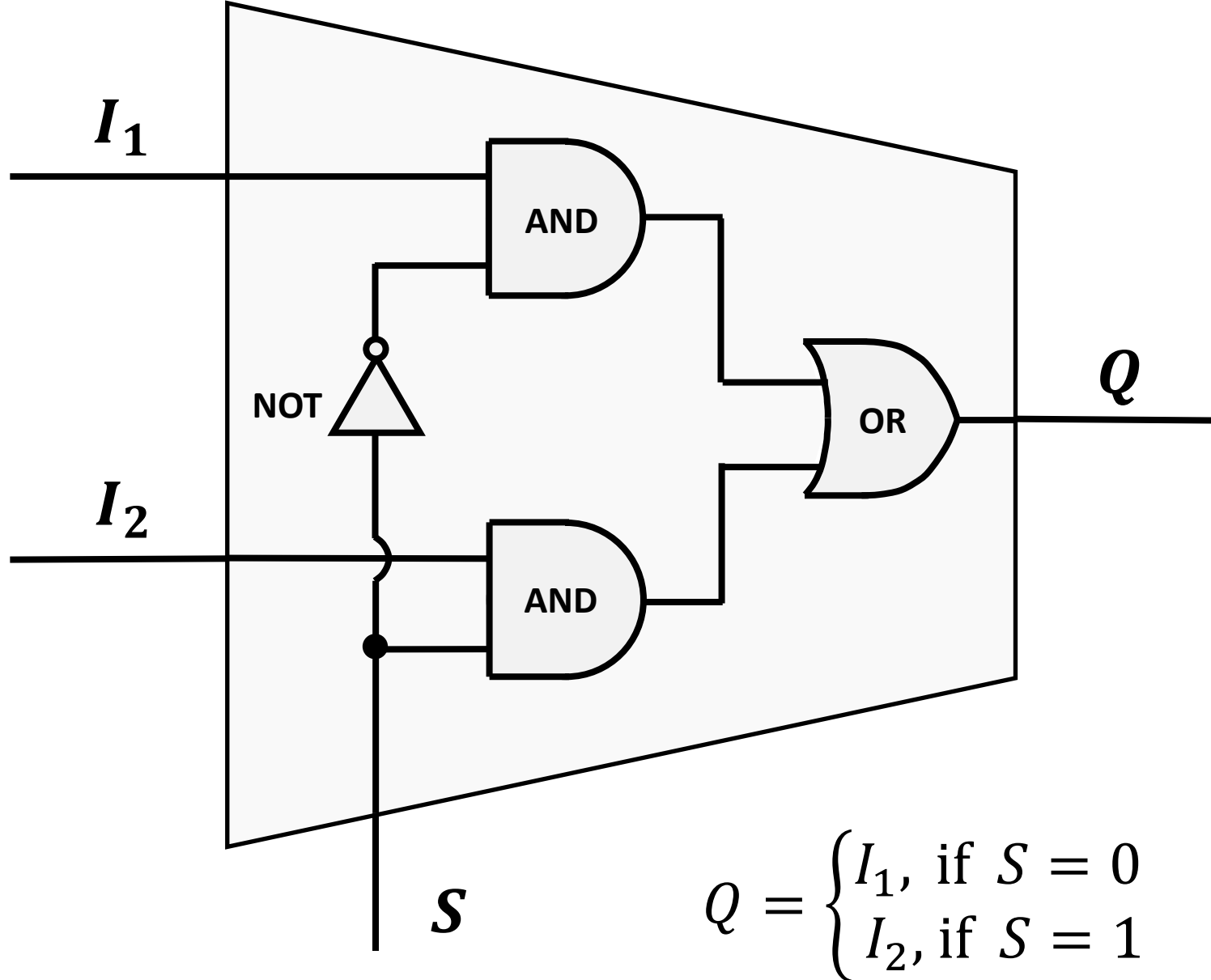
2-to-1 Multiplexer Implementation



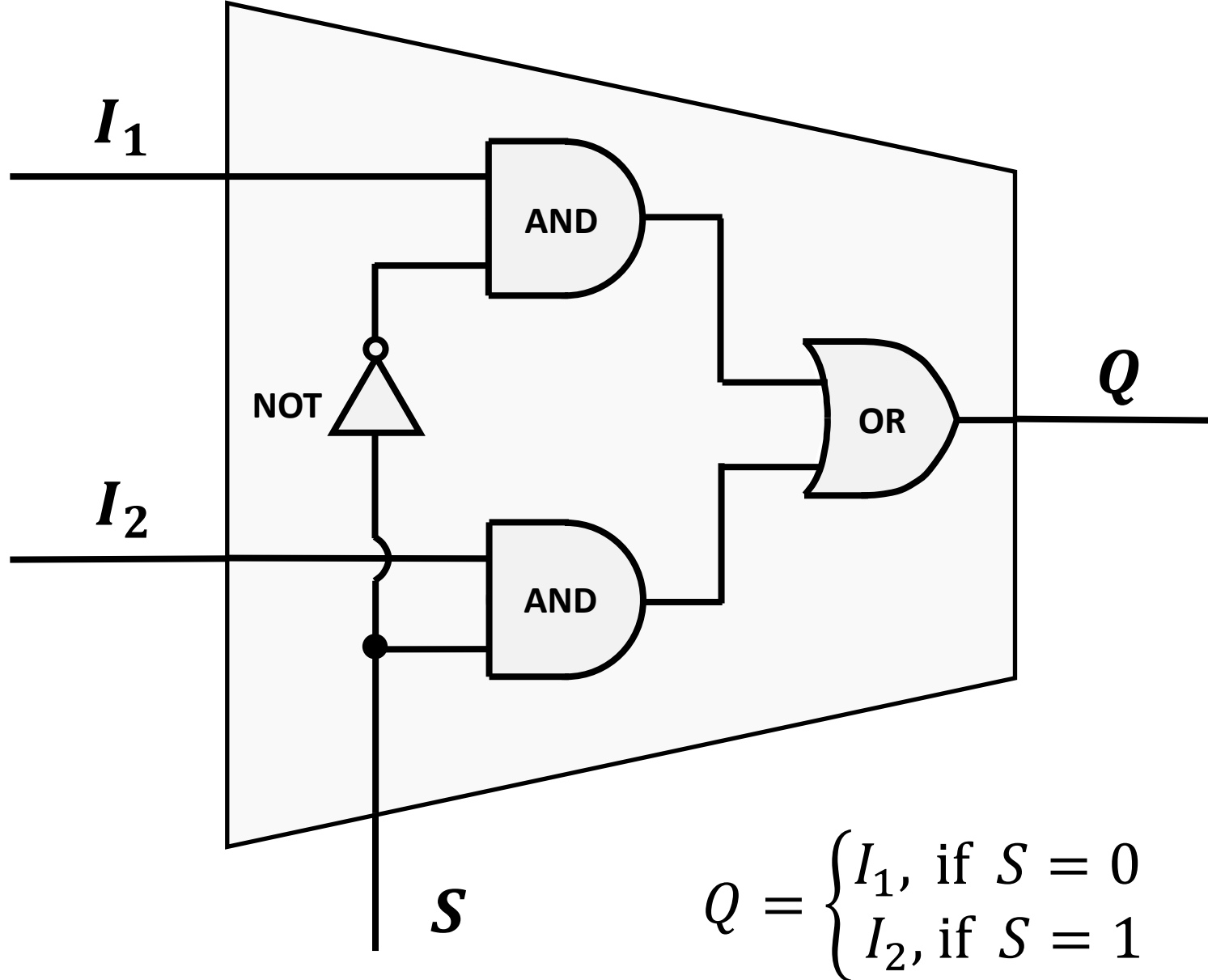
2-to-1 Multiplexer Implementation



2-to-1 Multiplexer Implementation



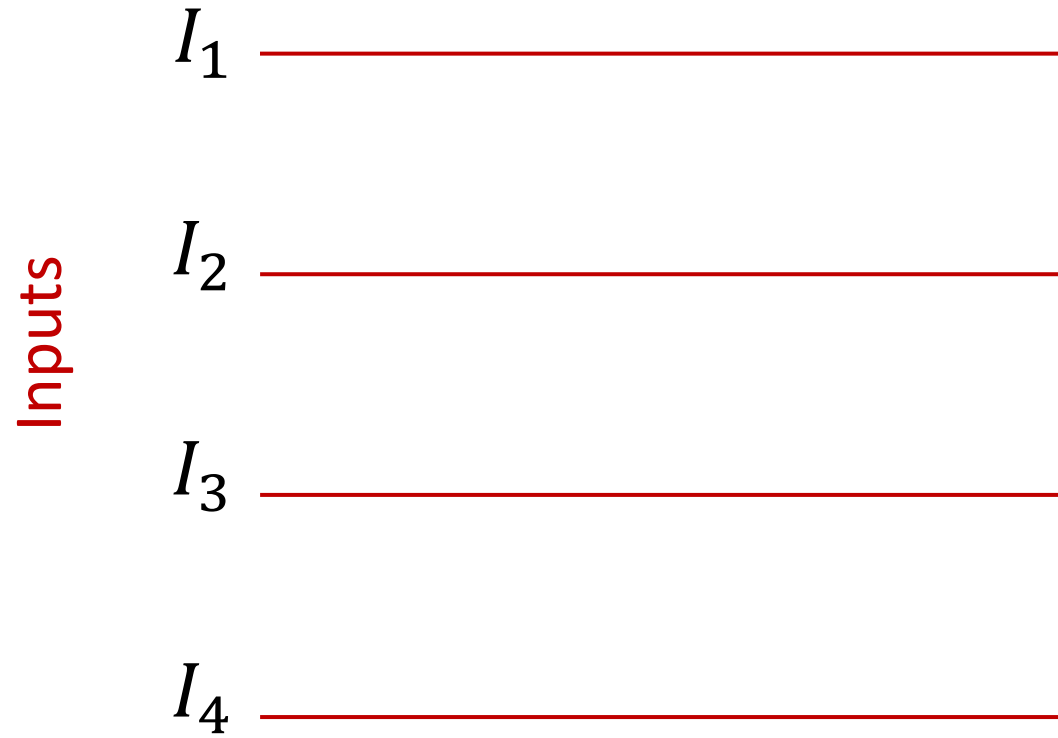
2-to-1 Multiplexer Implementation



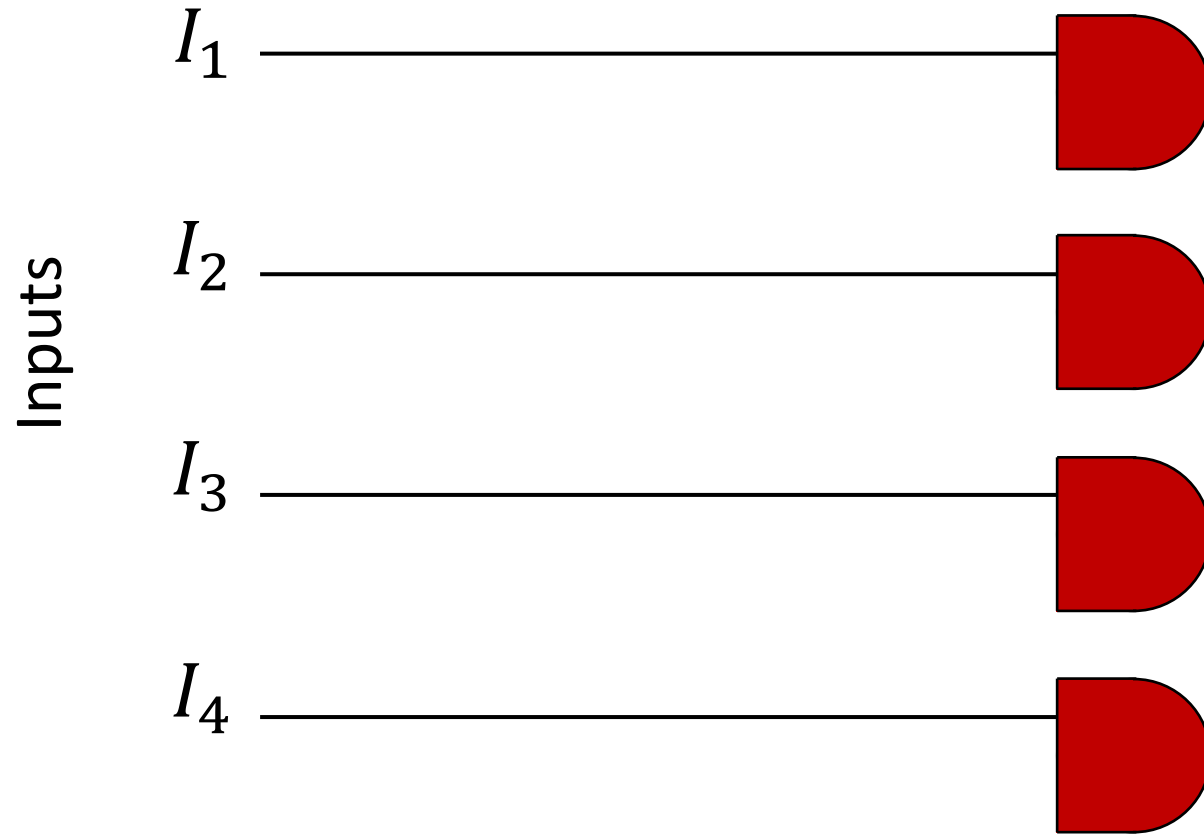
Verification of correctness:

I_1	I_2	S	Q
0	0	0	0
1	0	0	1
0	1	0	0
1	1	0	1
0	0	1	0
1	0	1	0
0	1	1	1
1	1	1	1

4-to-1 Multiplexer Implementation

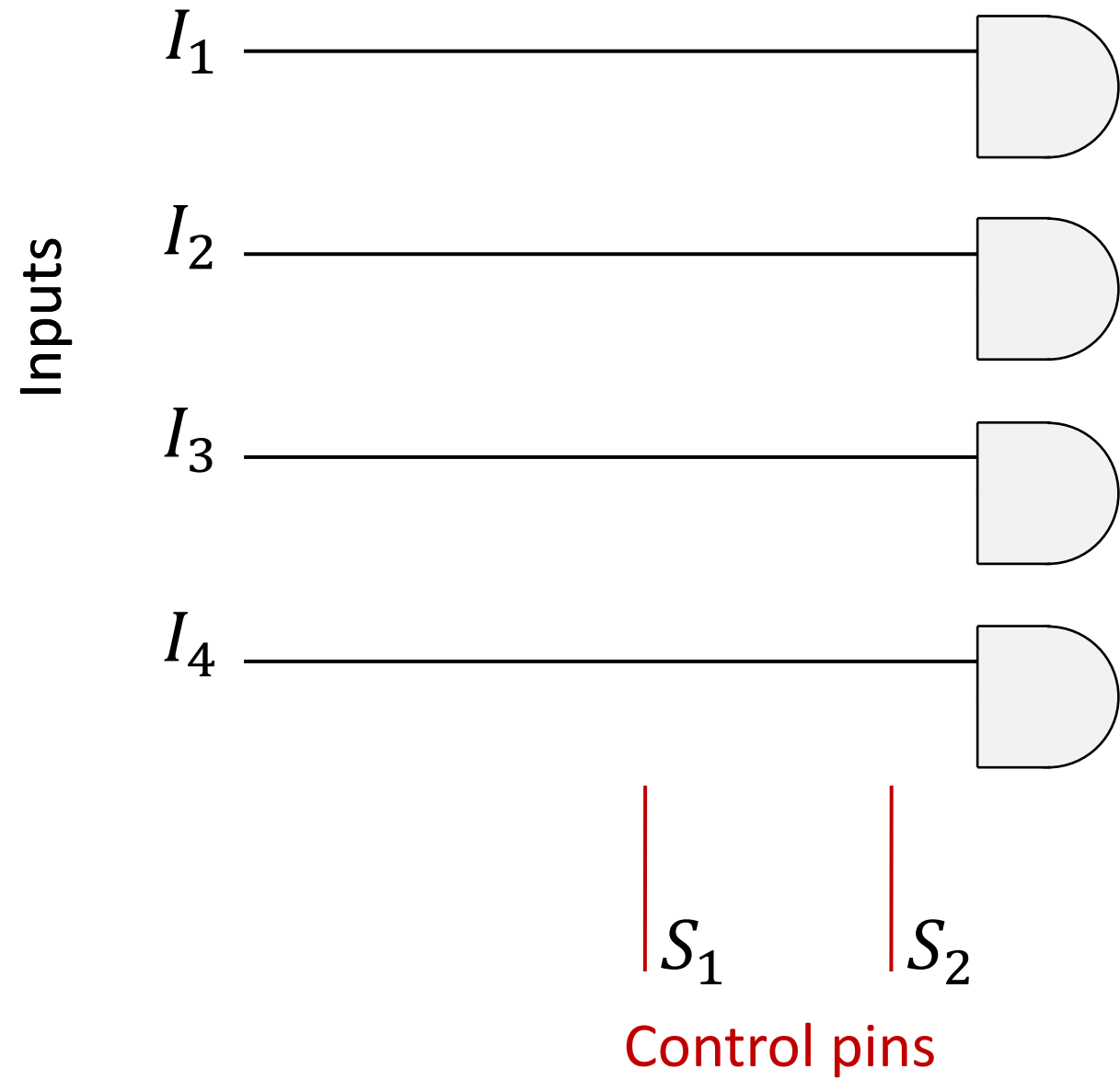


4-to-1 Multiplexer Implementation

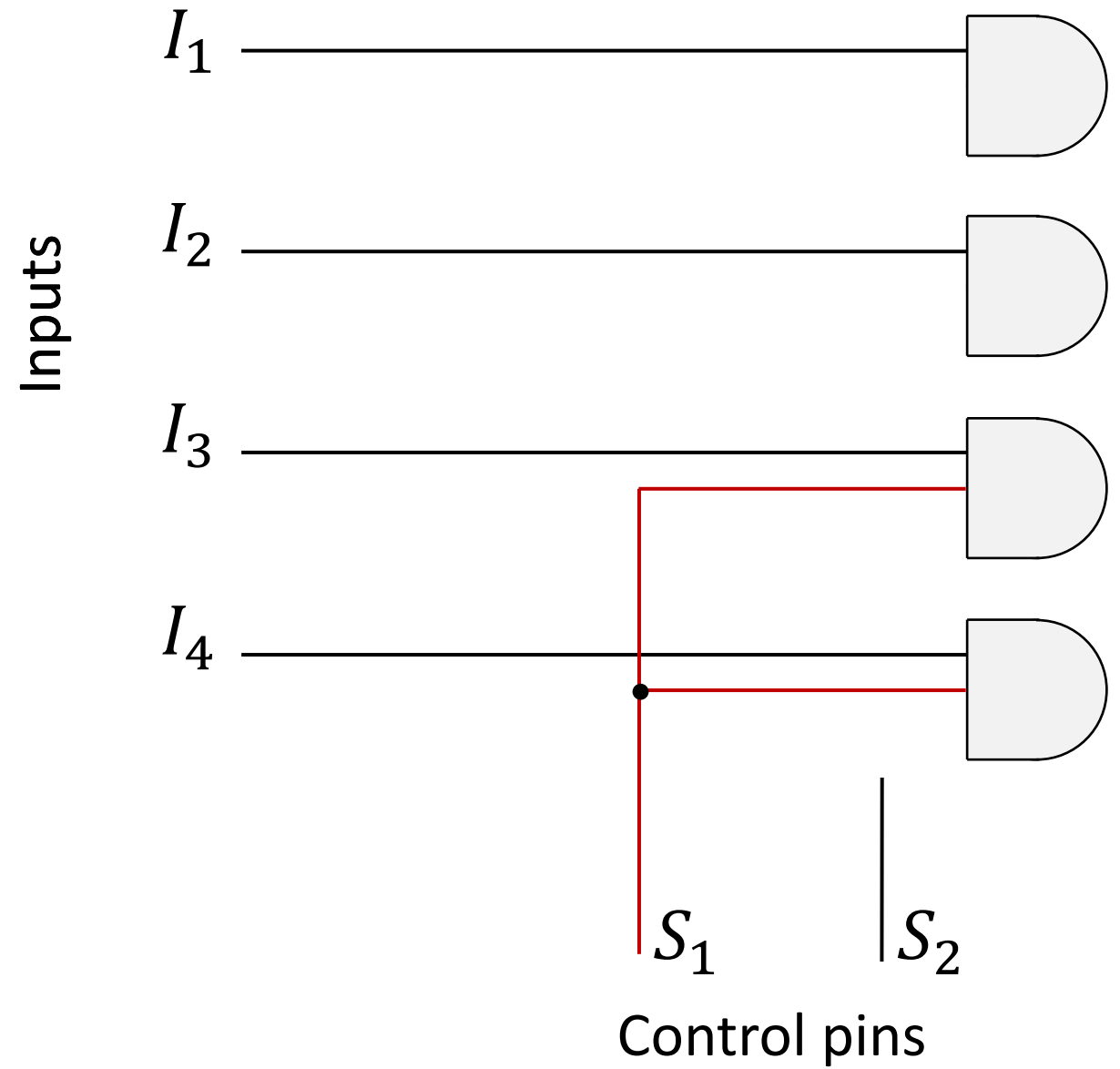


Each input pin is connected to
an individual AND logic gate

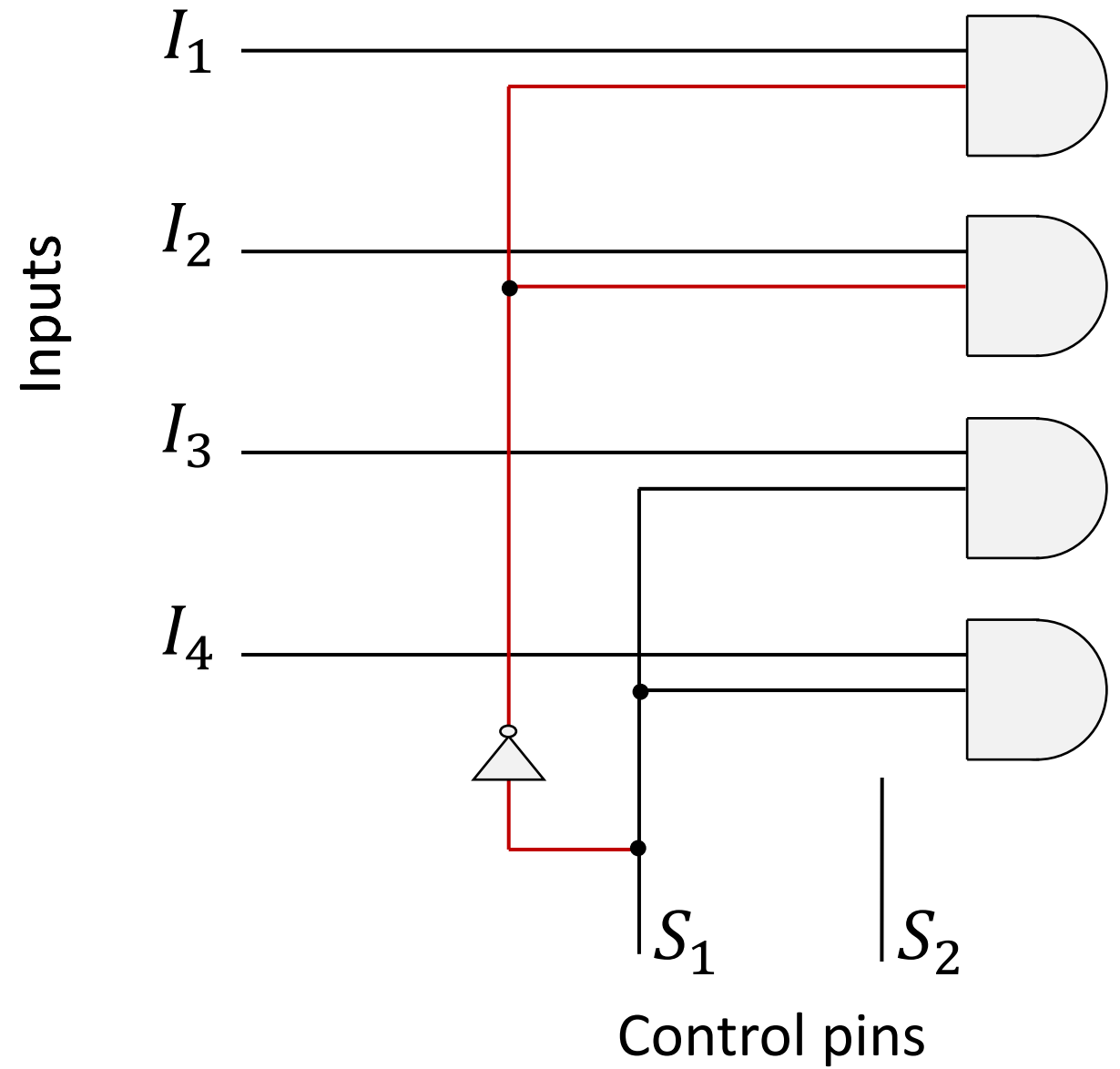
4-to-1 Multiplexer Implementation



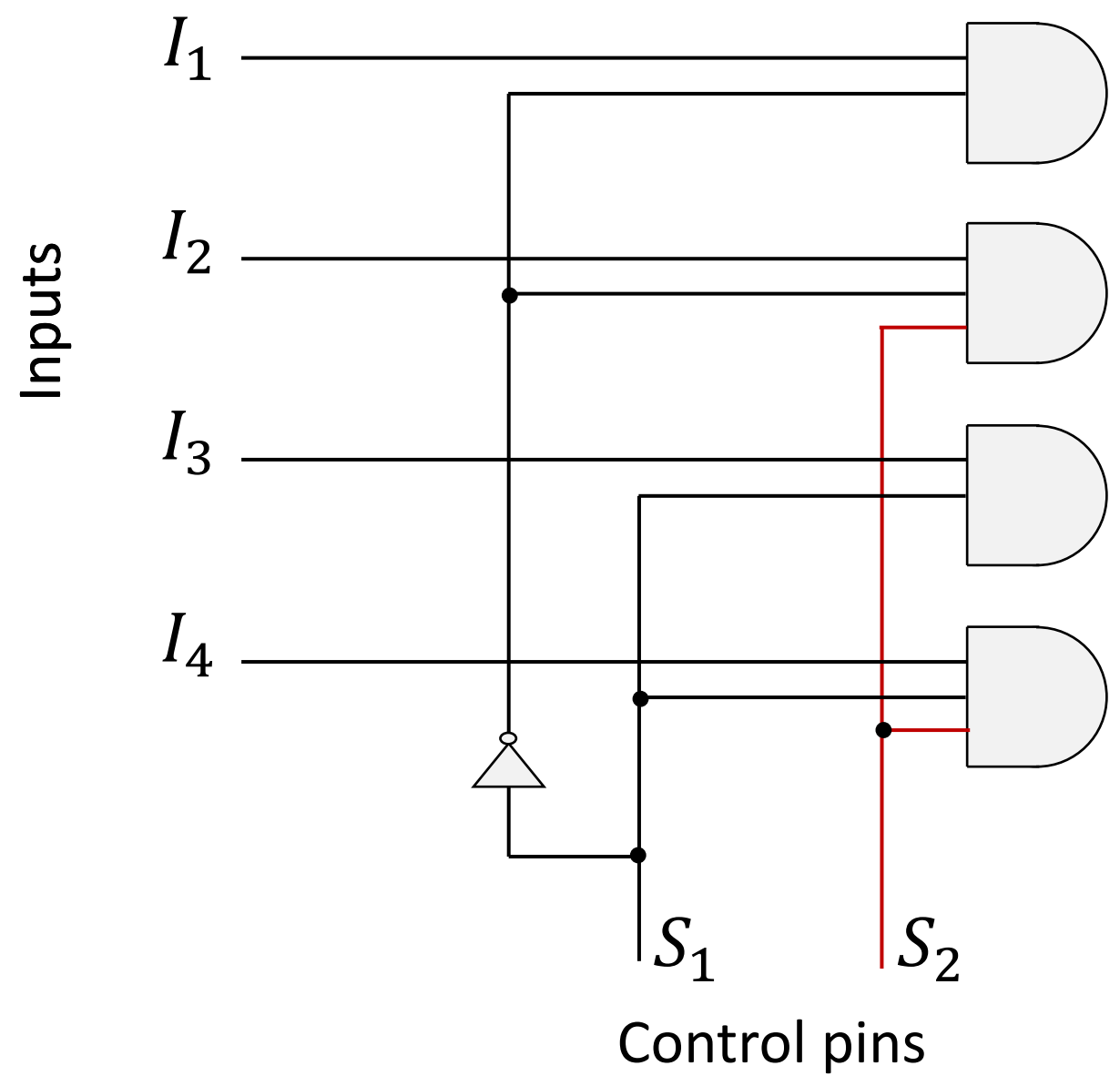
4-to-1 Multiplexer Implementation



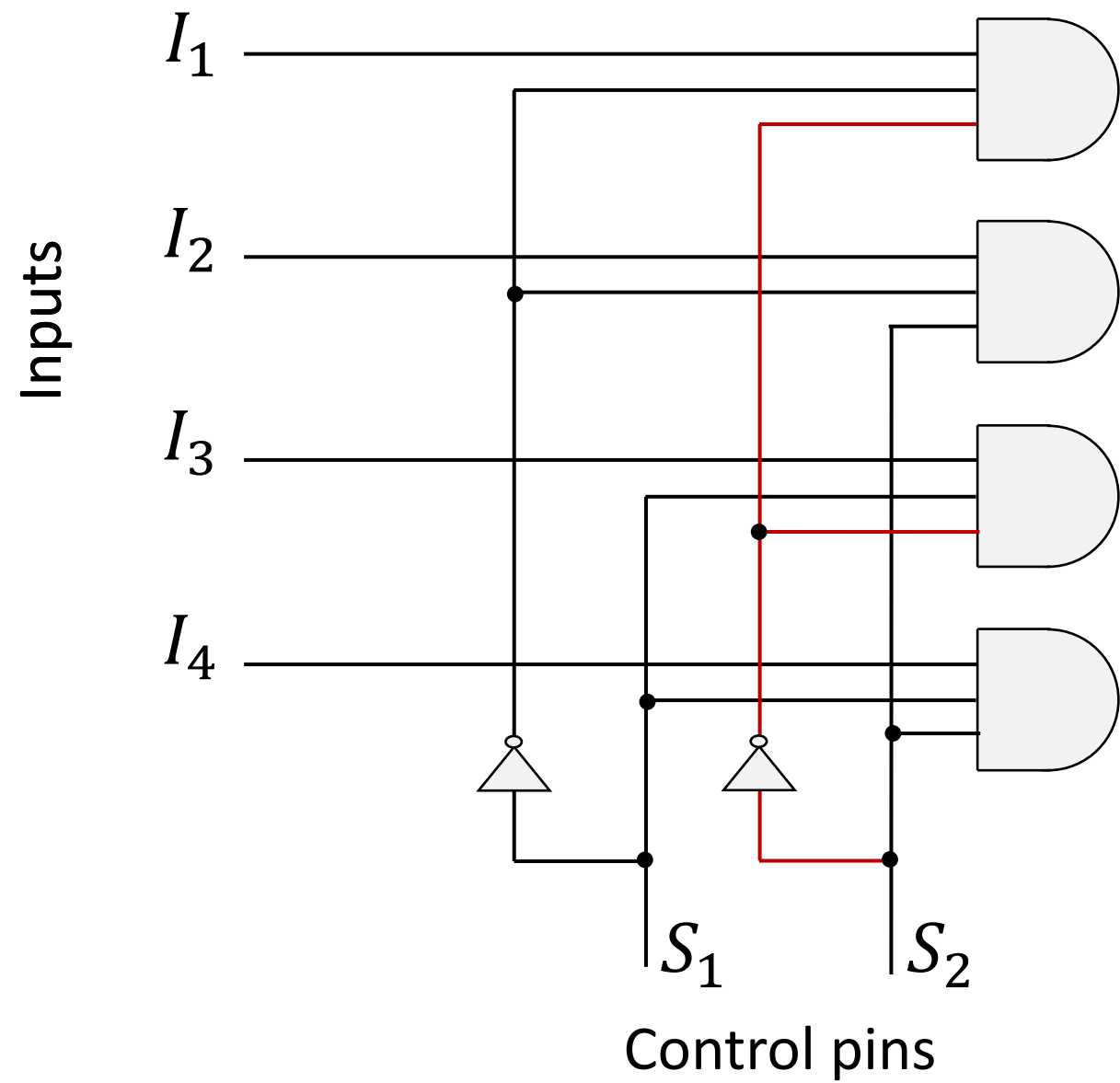
4-to-1 Multiplexer Implementation



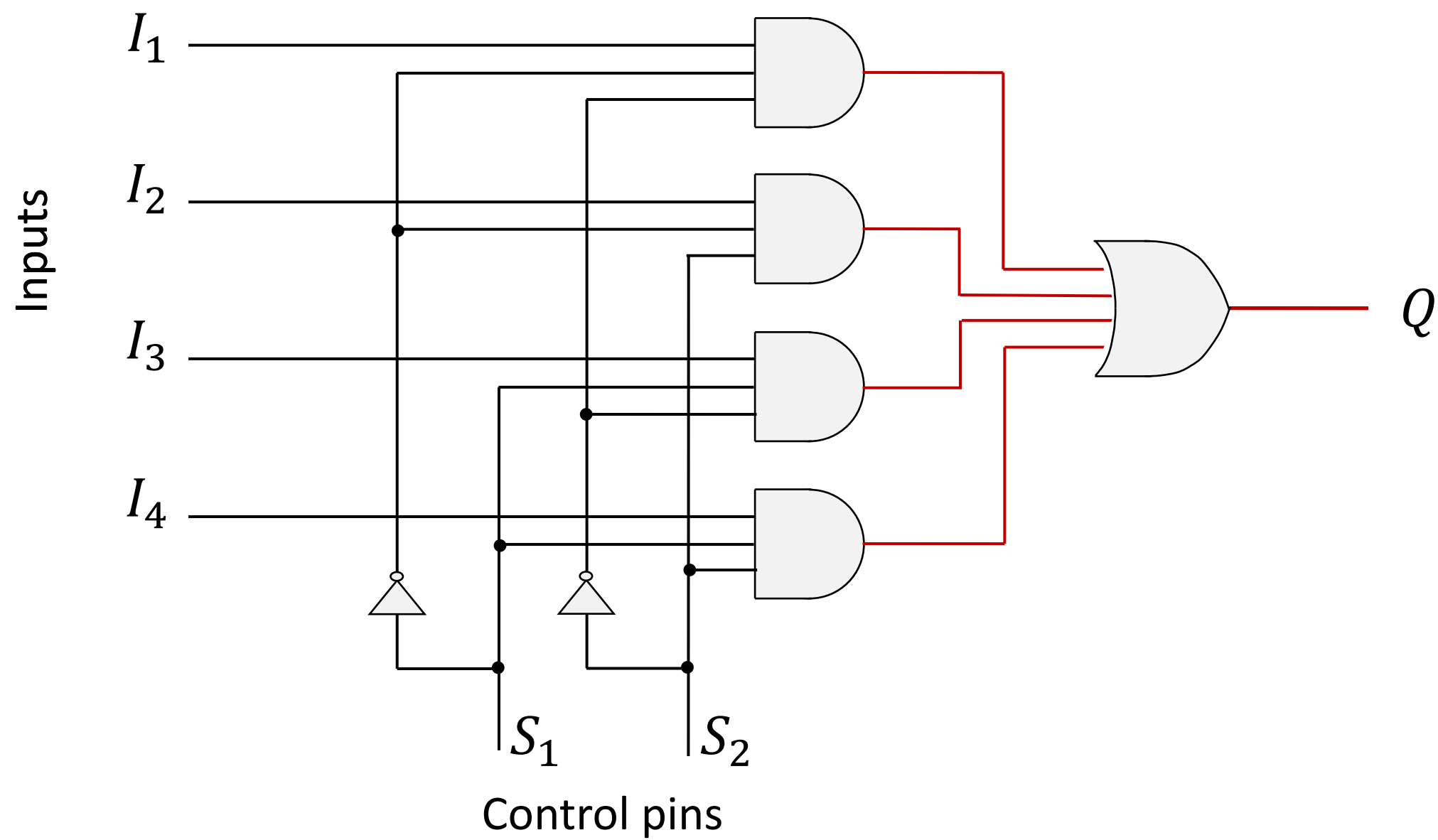
4-to-1 Multiplexer Implementation



4-to-1 Multiplexer Implementation

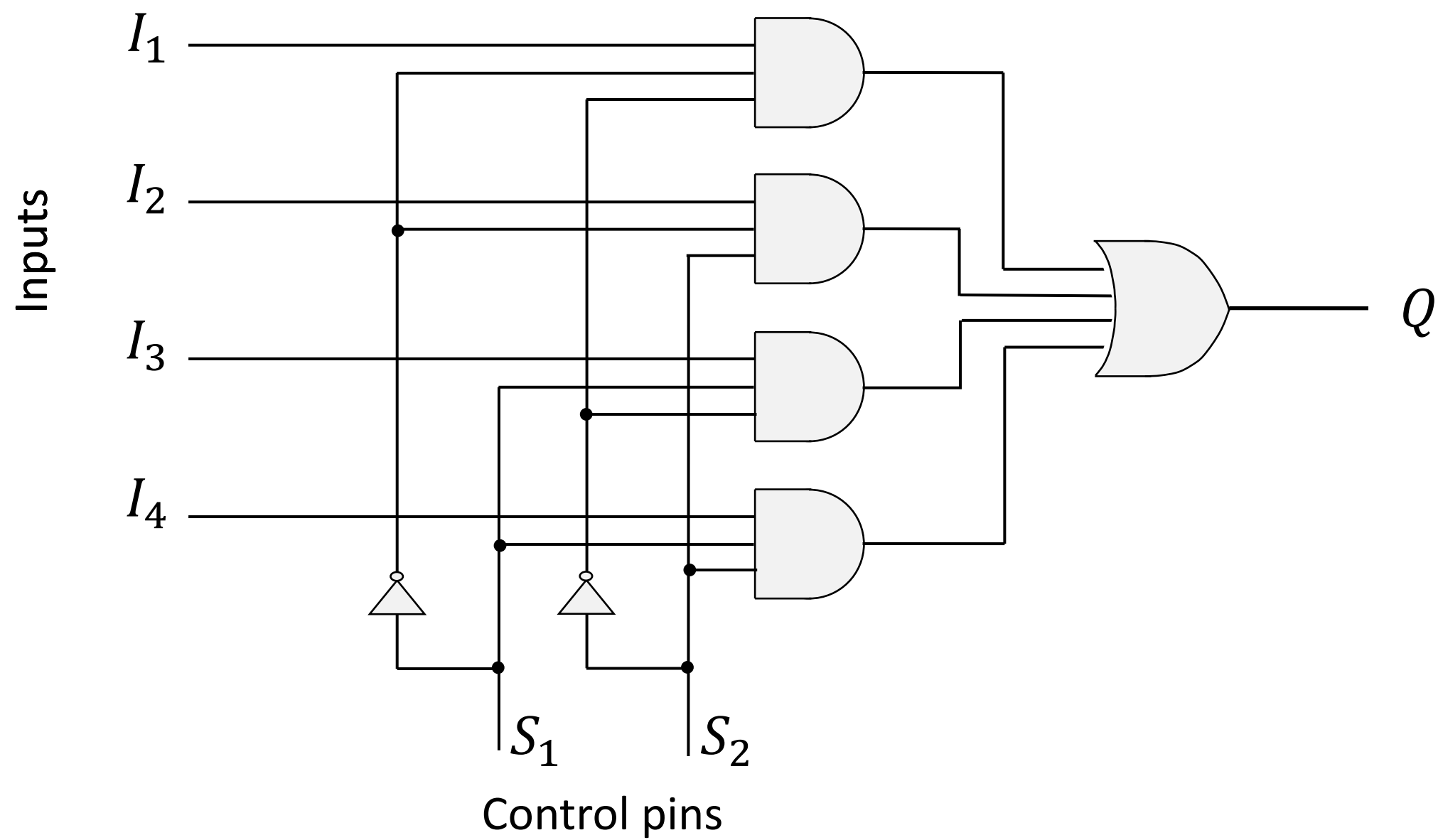


4-to-1 Multiplexer Implementation

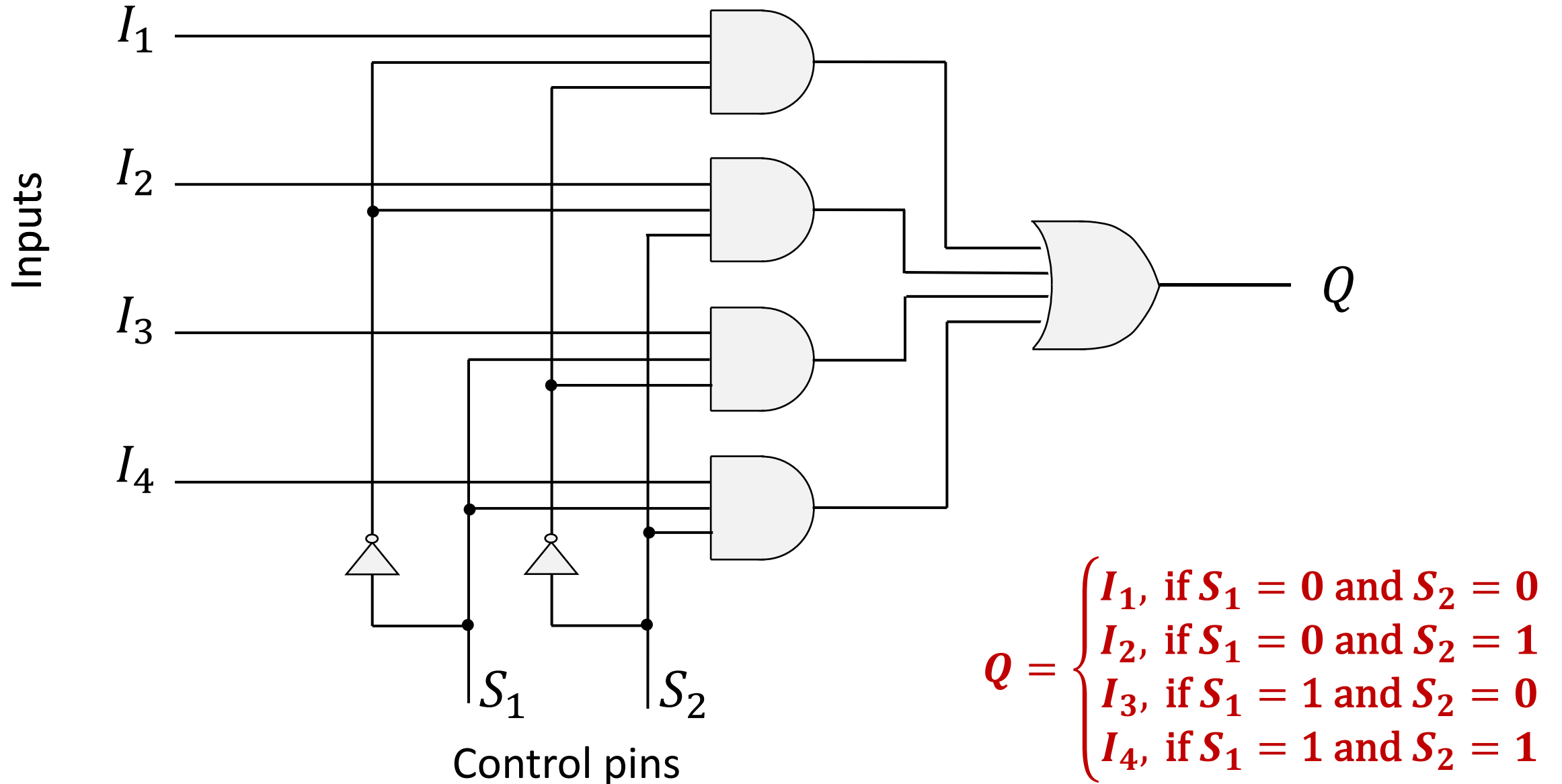


4-to-1 Multiplexer Implementation

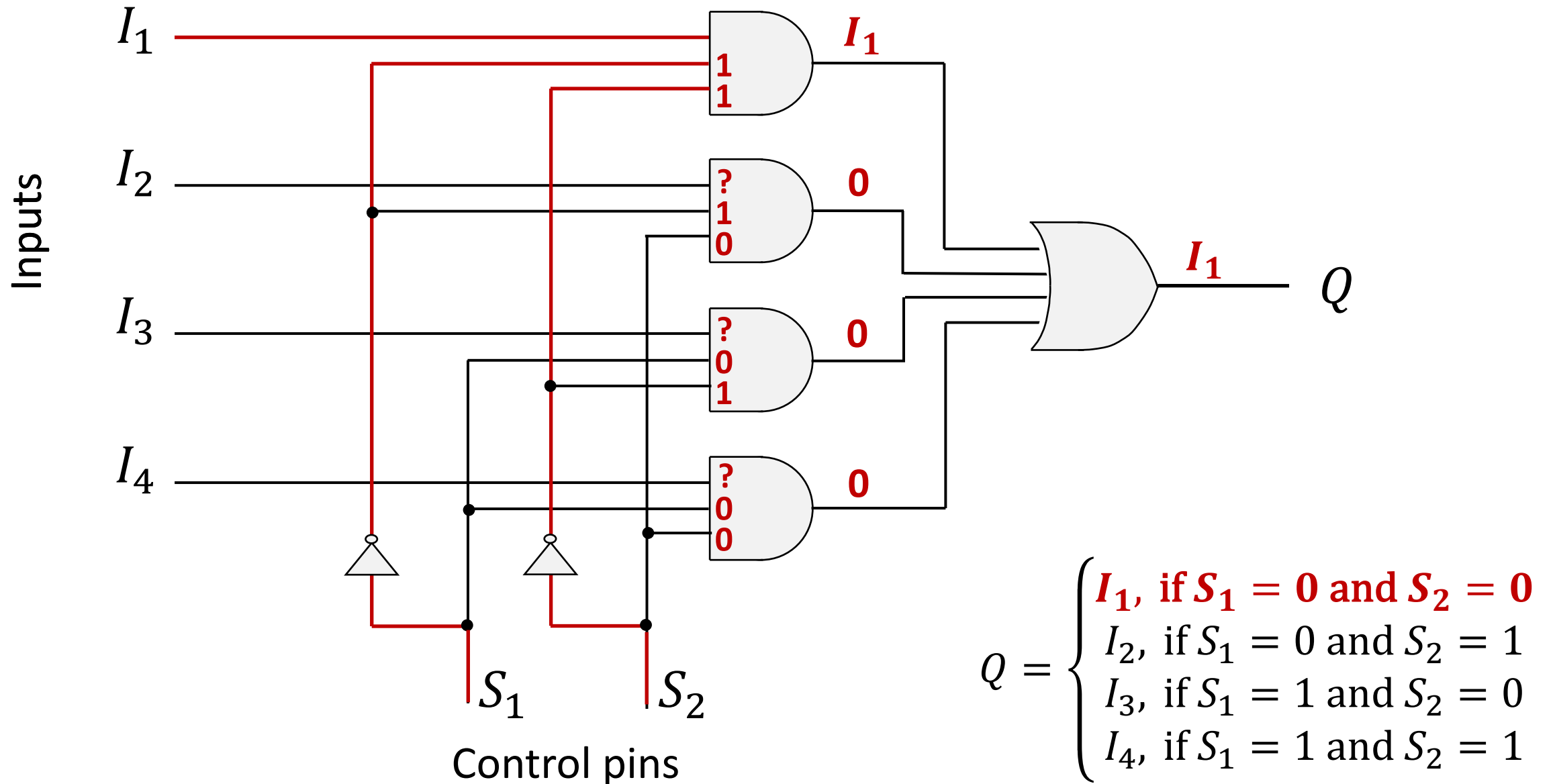
Based on S_1 and S_2 signals,
output Q is set to one of $I_1, \dots, I_4$ input pins



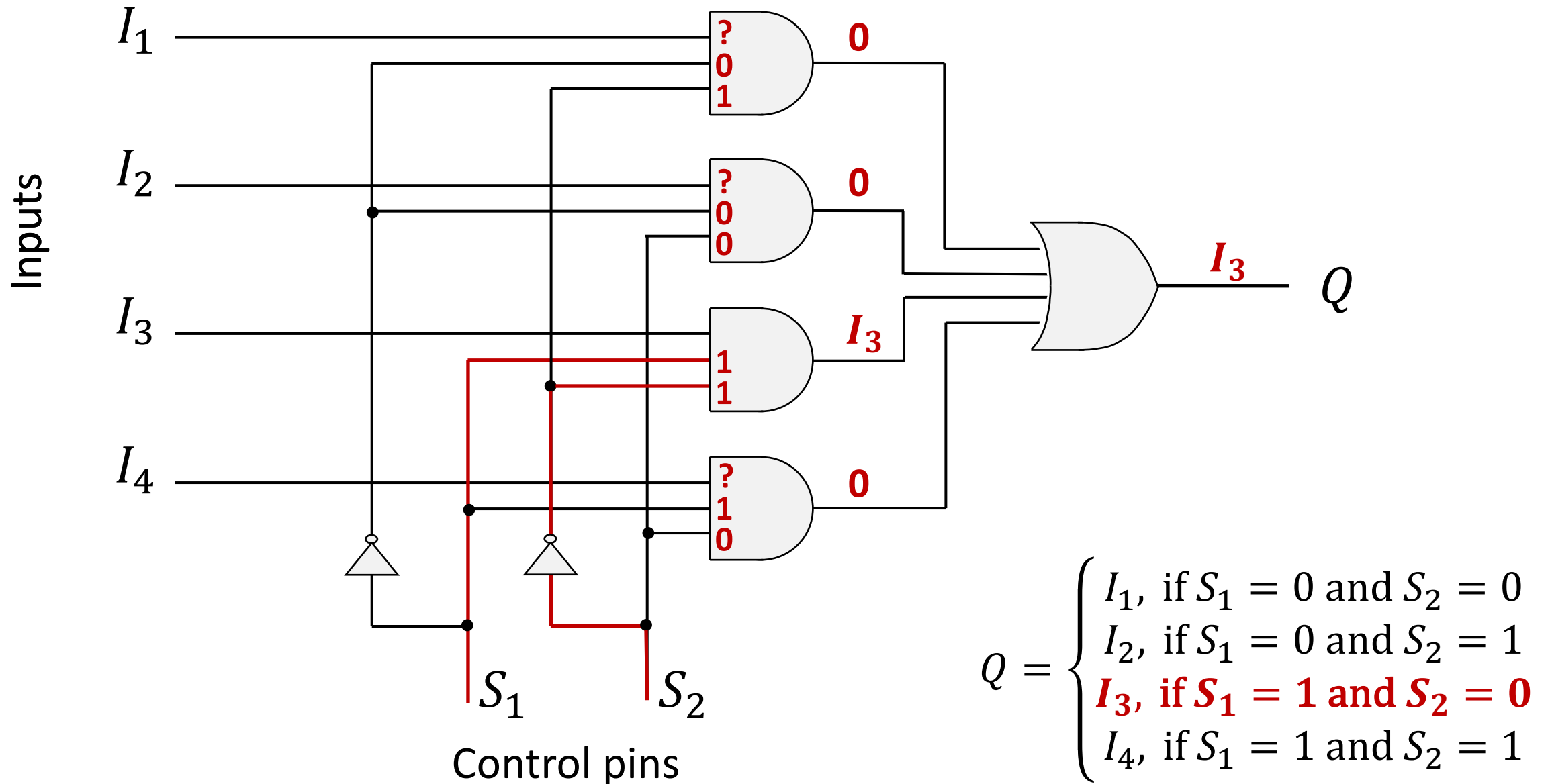
4-to-1 Multiplexer Implementation



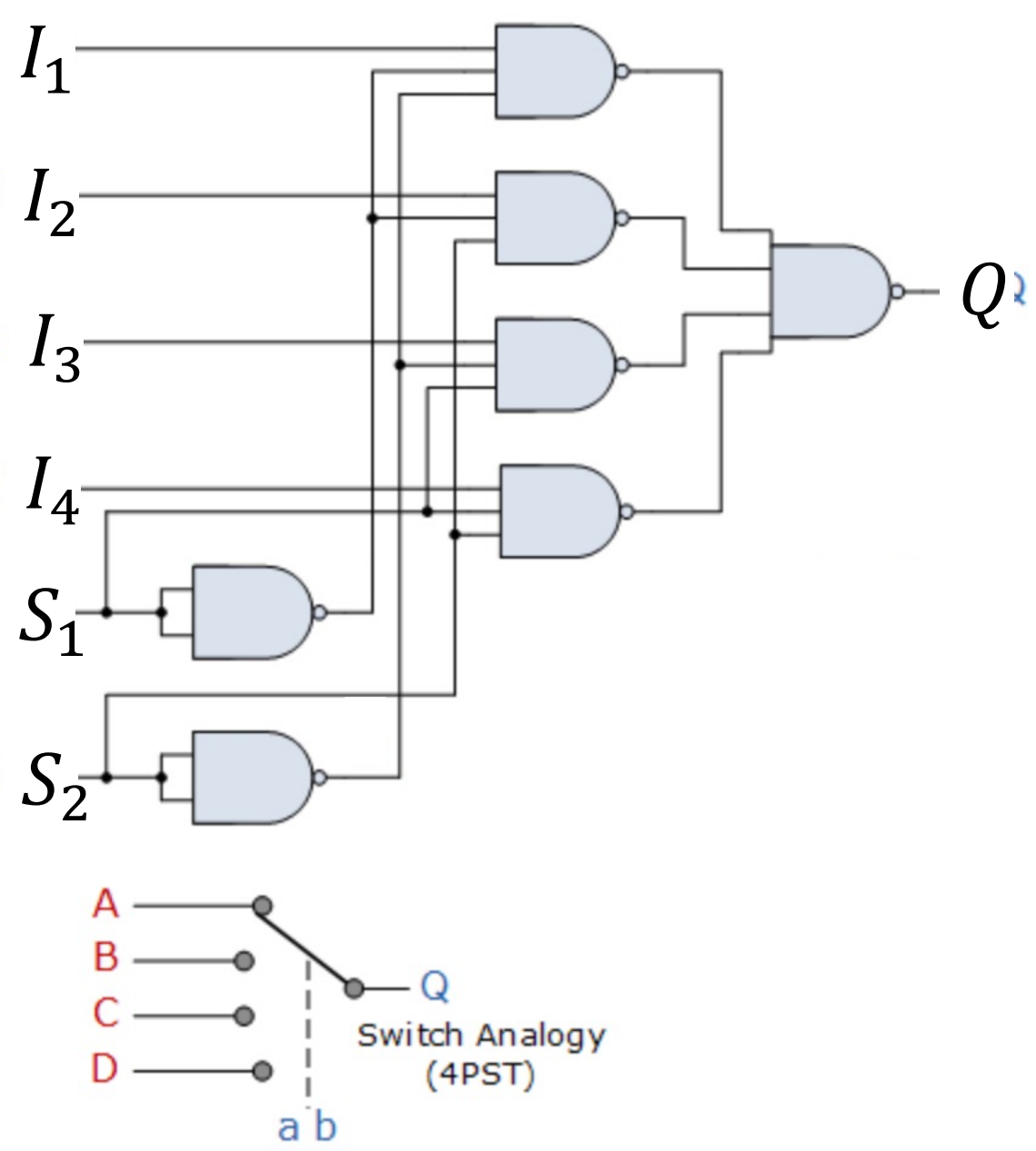
4-to-1 Multiplexer Implementation



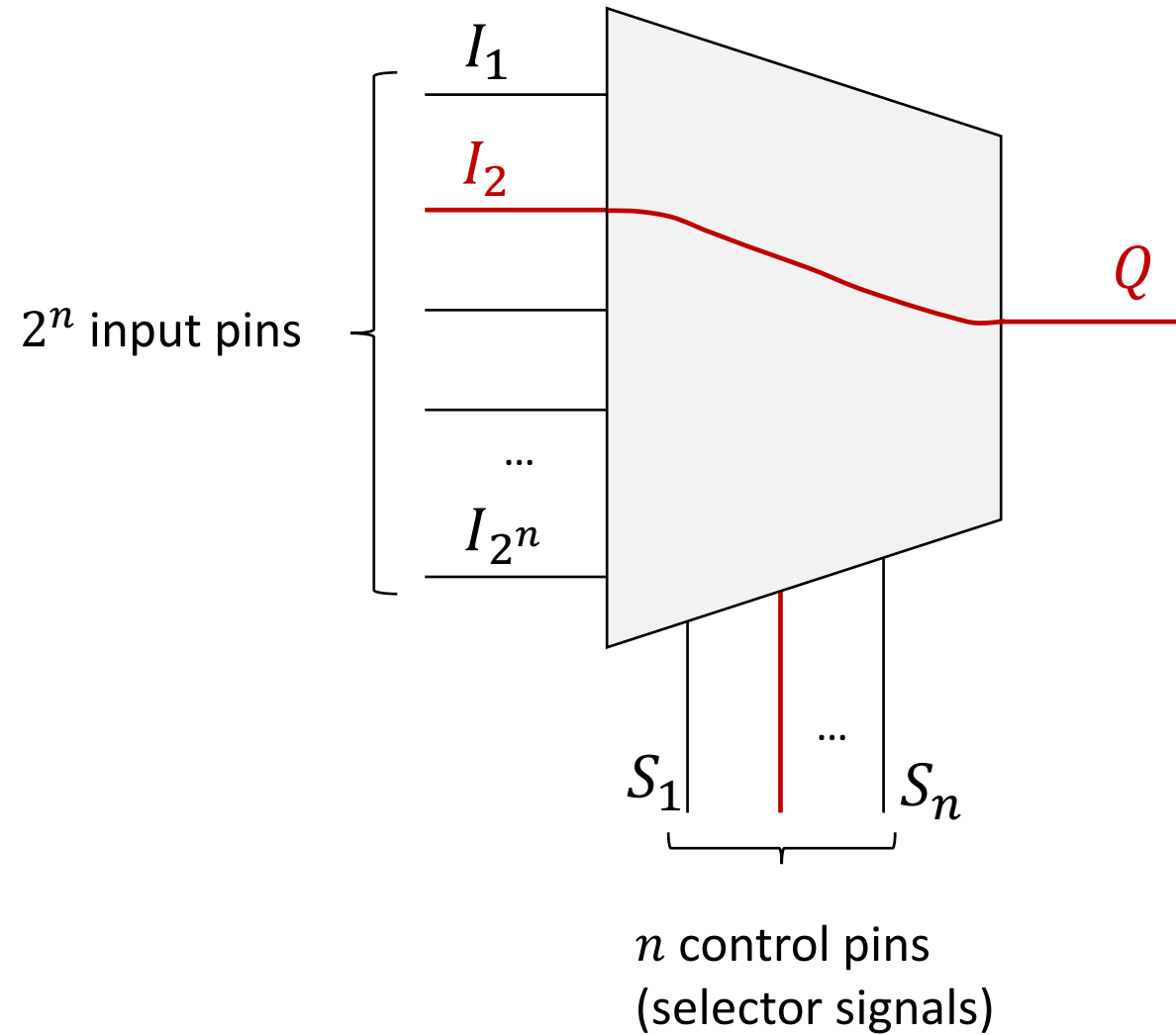
4-to-1 Multiplexer Implementation



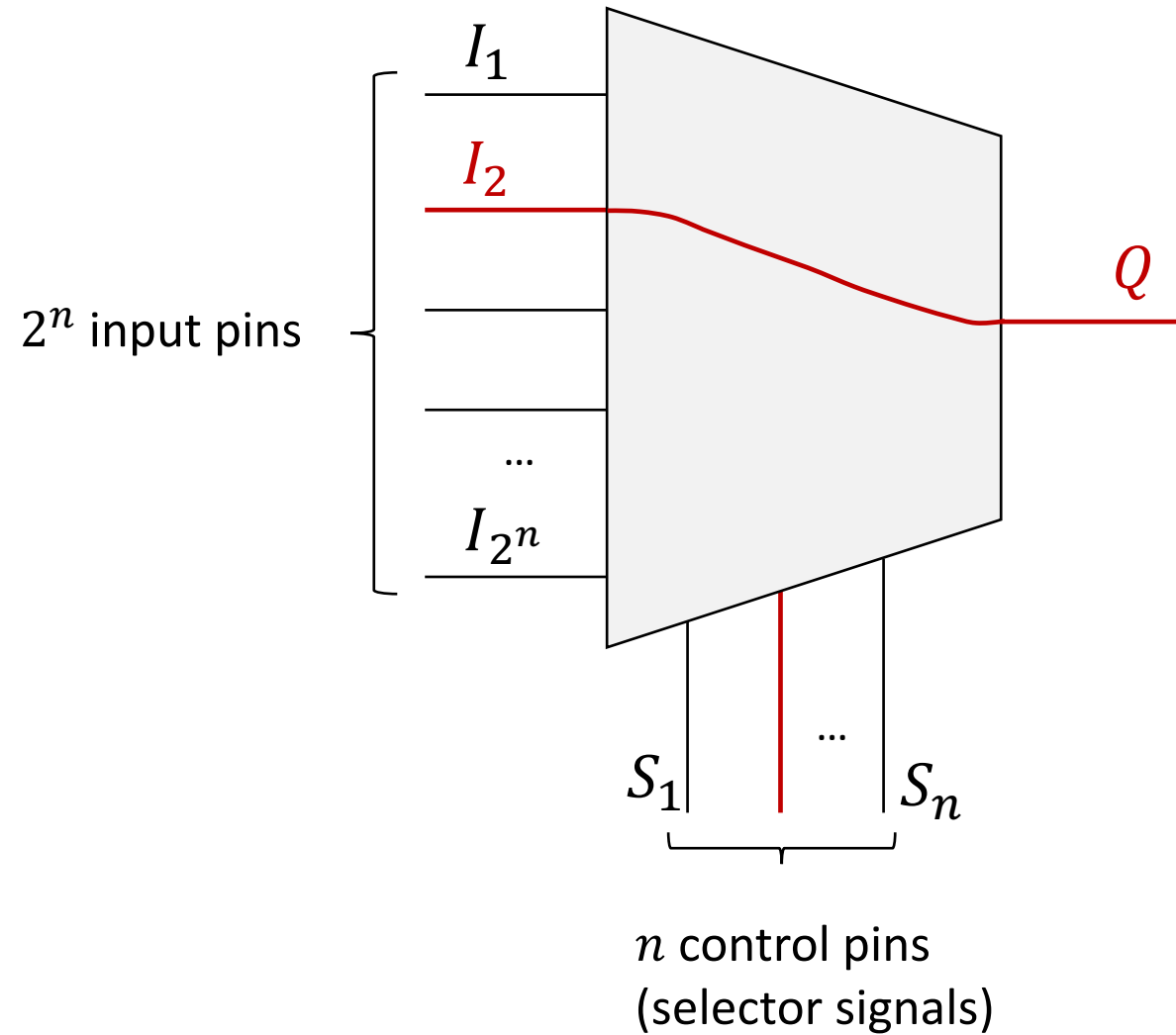
4-to-1 Multiplexer: Implementation through NAND (Universal) Gates



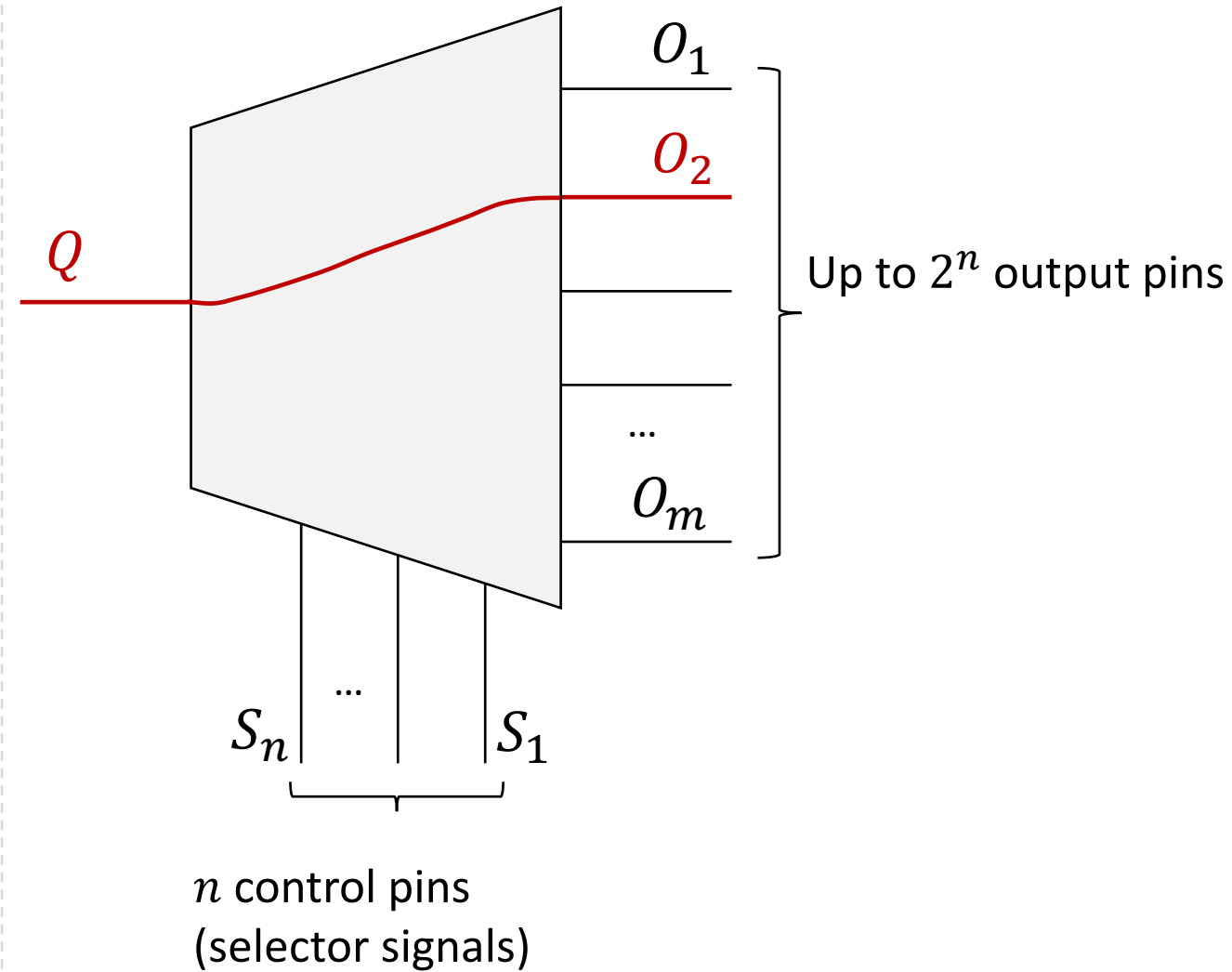
Multiplexer



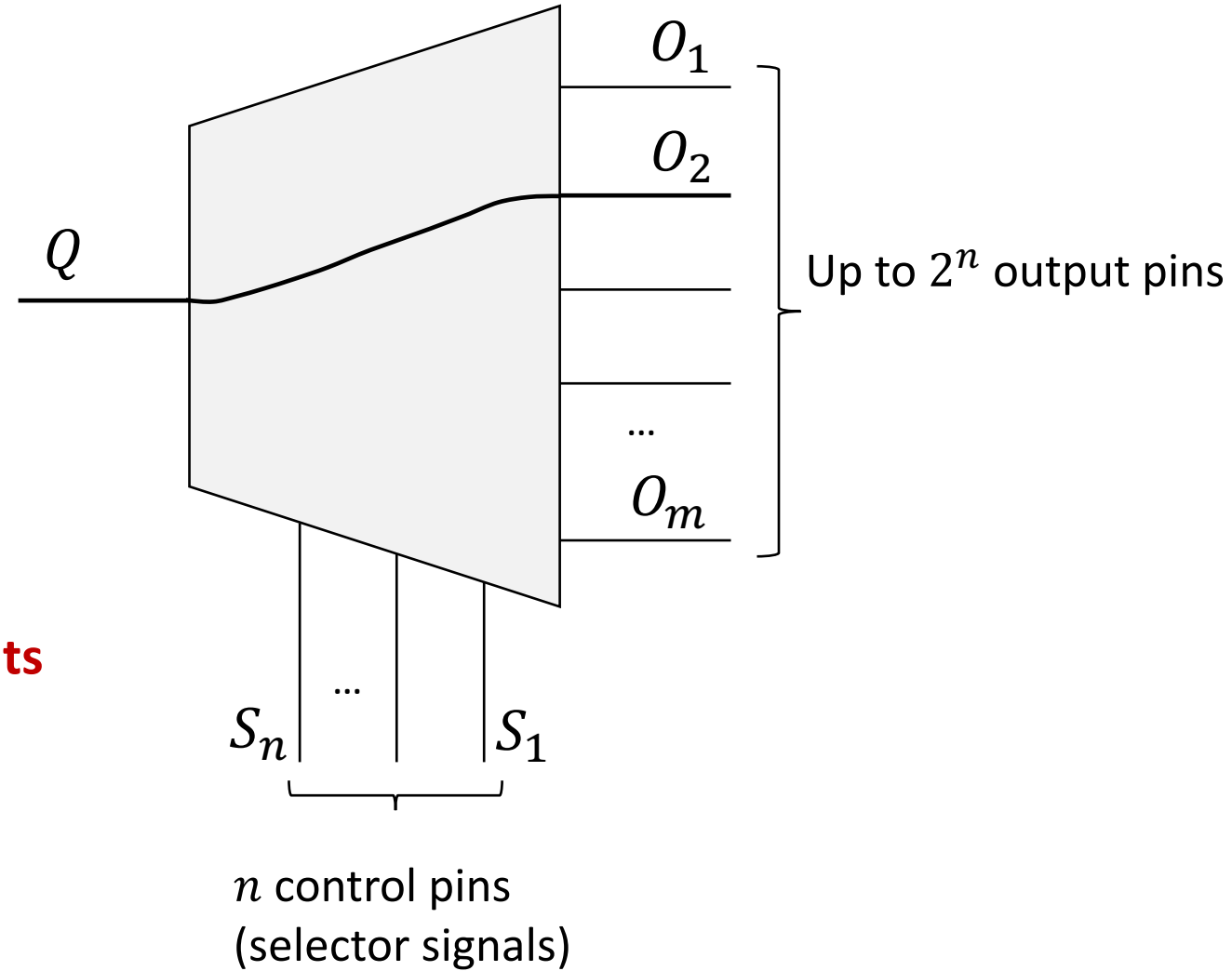
Multiplexer



Demultiplexer

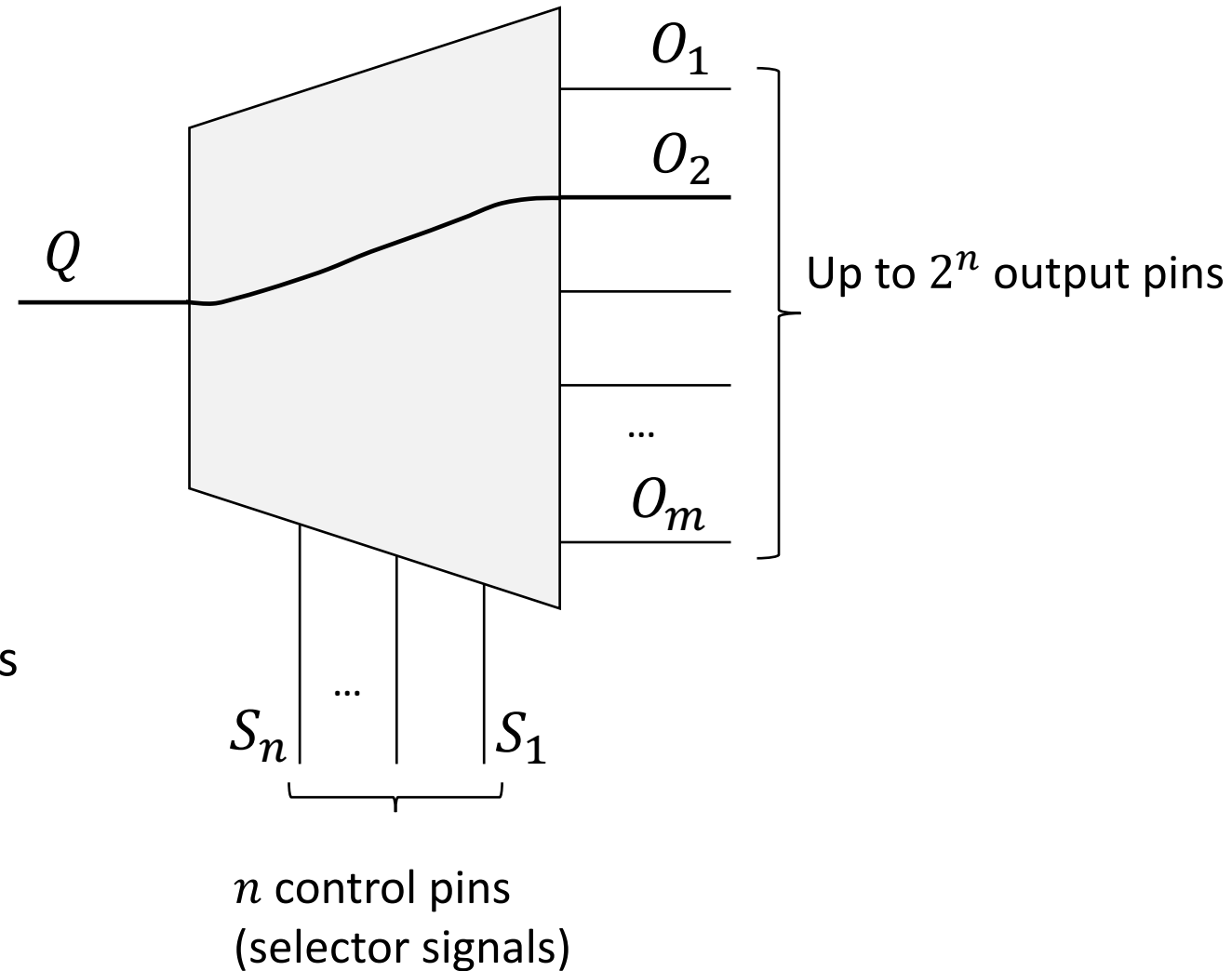


Demultiplexer



**Based on control pin signals,
demultiplexer sends its input to one of its outputs**

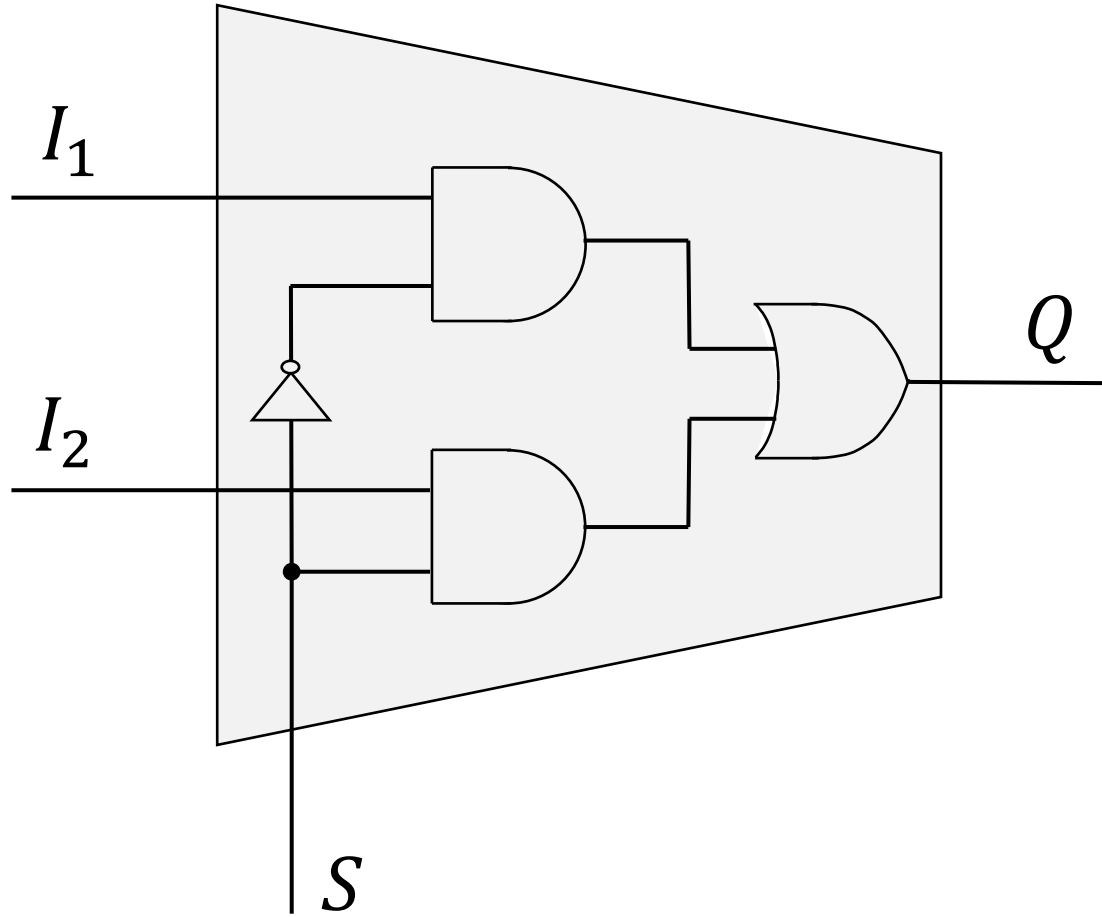
Demultiplexer



Based on control pin signals,
demultiplexor sends its input to one of its outputs

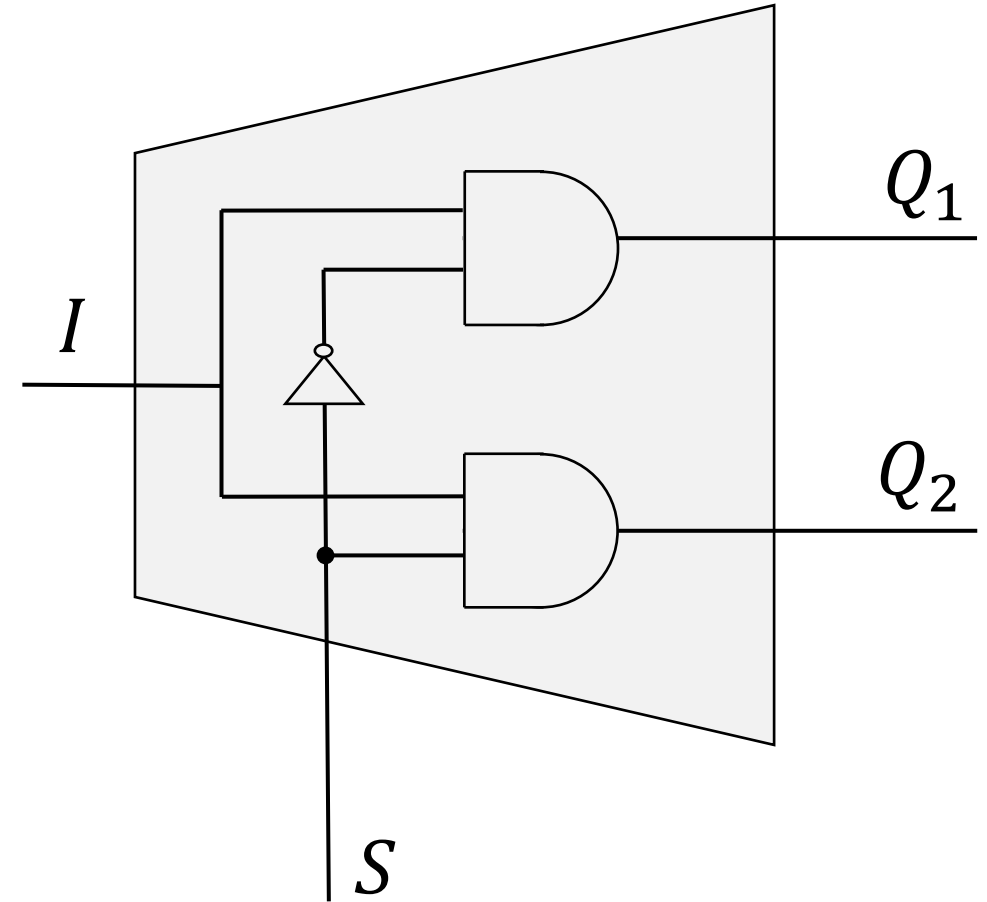
**All other outputs are set to some
default value (e.g. "0")**

2-to-1 Multiplexer



$$Q = \begin{cases} I_1, & \text{if } S = 0 \\ I_2, & \text{if } S = 1 \end{cases}$$

1-to-2 Demultiplexer



$$\begin{aligned} Q_1 &= I \text{ and } Q_2 = 0, & \text{if } S = 0 \\ Q_1 &= 0 \text{ and } Q_2 = I, & \text{if } S = 1 \end{aligned}$$