

Innopolis University
Academic Year 2023/2024
Midterm Exam of Computer Architecture
2nd November 2023

Student Full Name:

Student Group:

Grade Summary (for instructors fill)	
Question	Grade
Question 1	
Question 2	
Question 3	
Question 4	
Question 5	
Question 6	
Question 7	
Question 8	
Total	

Maximum score: 12 points

Please write clearly your name and your solutions. What will not be understood will be considered wrong. All answers must be provided in English.

This is a closed-book exam. You are not allowed to use any reference materials or electronic equipment, apart from this booklet and pens. You are not allowed to consult any person, otherwise you will be disqualified from this exam at the very first attempt.

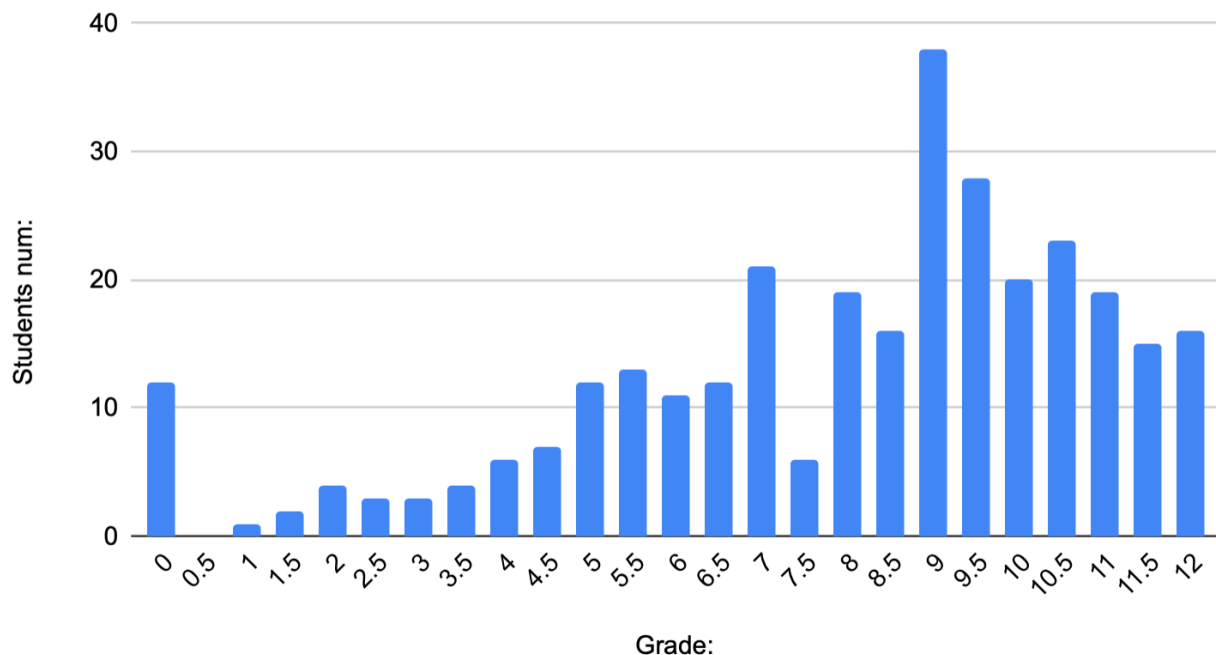
Good Luck!

Signature:

Student Full Name:

Grades Distribution:

Students num: vs. Grade:



Question 1. (1 point) Processor A has 4 cores of 2.3 GHz frequency each, processor B has 2 cores of 2.1 GHz each, and processor C has 4 cores of 2.2 GHz each. Which processor has an “overall better performance” from a theoretical perspective?

- a) **Processor A (correct)**
- b) Processor B
- c) Processor C

Note on grading:

The only correct option chosen – 1 point, otherwise 0

Question 2. (1 point) What is the major objective of a pipelined execution for processor instructions?

- a) To increase reliability through redundancy
- b) To facilitate performance by speculative execution
- c) To resolve underflow exceptions
- d) **To speed-up an overall program execution (correct)**
- e) To increase the energy consumption
- f) To facilitate the use of two’s complement notation for signed numbers
- g) No choice is correct

Note on grading:

Correct option “d” chosen – 1 point, and for every incorrect option, except “g”, penalty (-0.2) points. If option “g” chosen – 0.

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Question 3. (1 point) Fill-in the following comparison table for S/R latch and D flip-flop circuits:

Criteria	S/R latch	D flip-flop
Storage capacity (in bits)	1 bit	1 bit
Output synchronization with clock (write "yes" or "no")	NO	YES
Power consumption (write "higher" or "lower")	LOWER	HIGHER

Note on grading:

Mistakes in "Output synchronization..." or "Power consumption..." rows – penalty of (-0.5) for each row. Mistakes in "Storage capacity..." – penalty of (-0.5) for each cell with incorrect value.

Question 4. (1 point) Convert decimal value "-14" into 8-bit two's complement notation for representing signed numbers. It is mandatory to illustrate the key computation steps in the "solution" field.

Answer:

1	1	1	1	0	0	1	0
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Note on grading: ALL cells of the "Answer" field (the question requires to provide the answer in 8-bit format) are filled with correct values (8 bits in total) and the solution is provided – 1 point, in any other case – 0.

Solution (mandatory):

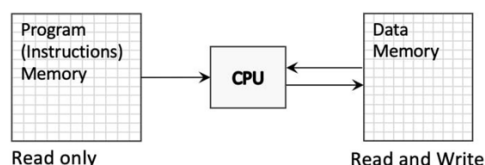
- Find the binary representation of 14: 00001110
- Invert the bits (Change 0s to 1s and 1s to 0s): 11110001
- Add 1 to the result: 11110010

Question 5. (2 point) What is the key difference between Von Neumann and Harvard computer architectures? Illustrate with diagrams.

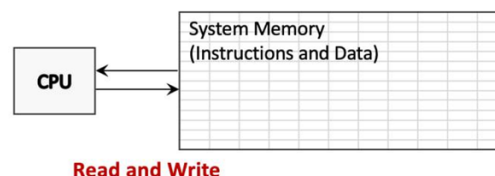
Answer:

The key difference is the following: Harvard architecture assumes two separate memory units: one – for program instructions, and one – for program data, while Von Neumann architecture assumes the same memory unit to be used for program instructions and data.

Harvard Architecture:



Von Neumann Architecture



Note on grading:

For both architectures correct diagrams with comprehensive labeling is provided – 2 points;

No diagrams are provided, but the difference is described correctly in words – 1 point;

Mistake of any type – penalty of (-1) point;

Otherwise 0 points

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Question 6. (2 points) Name at least 4 key differences between CPU and FPGA chips.

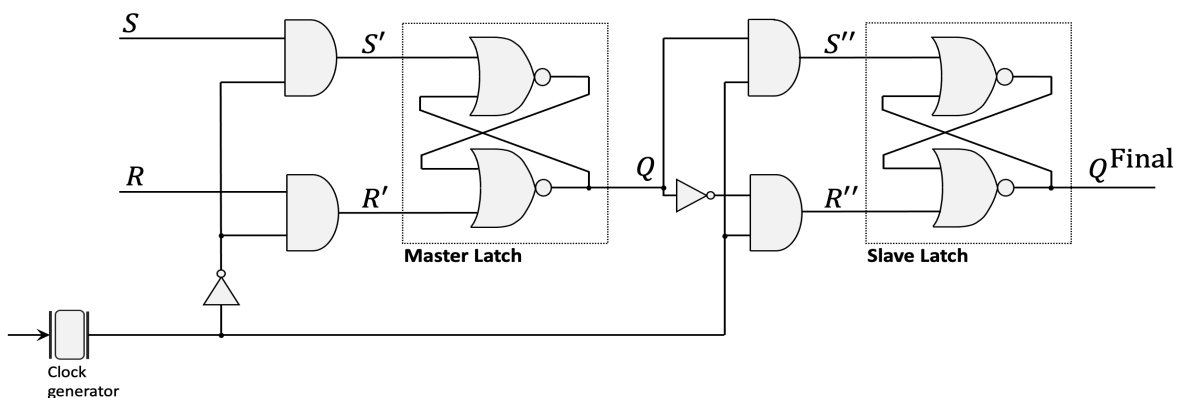
Some possible answers are the following:

Criteria	General-Purpose Processor	FPGA
Programmability	Cannot be reprogrammed	Reprogrammable
Instruction Set	Set of supported instructions cannot be changed	You define supported instructions yourself, by designing logic circuits
Computation Speed	Typically much slower	Faster
Power Consumption	Less	Significant power leakage
Price	Cheaper	More expensive (depends on FPGA "size": the number of Logic Elements, LE)

Notes on grading:

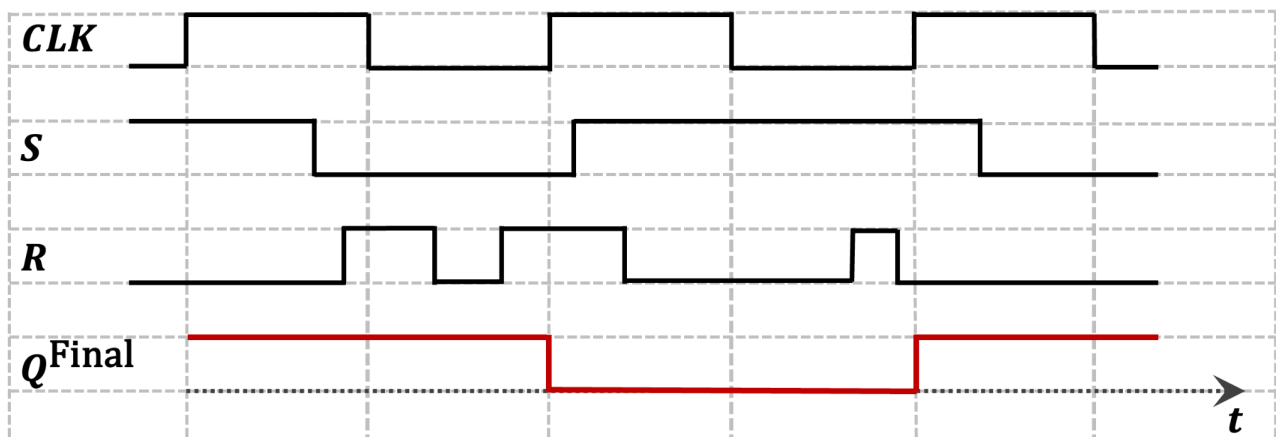
Every correct (out of 4) comparison is 0.5 points, and partially incorrect formulation is 0.25 points

Question 7. (2 points) Consider the following logic circuit:



Draw the signal curve in the timing diagram below for Q^{Final} output pin:

Answer:



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Notes on grading:

A fully correct diagram – 2 points;

As well as these only two diagrams are considered as partially correct and graded with 1 point:



Question 8. (2 points) Provide the logic circuit of 2-to-4 decoder by using AND and NOT logic gates. Describe such a logic circuit design in Verilog HDL

Logic circuit design	Verilog HDL implementation
The logic circuit diagram shows two input lines, I_1 and I_2, on the left. There are four output lines on the right, labeled O_1, O_2, O_3, and O_4. Each output is connected to an AND gate. The inputs to the AND gates are as follows: O_1 is connected to I_1 and $\text{NOT}(I_2)$; O_2 is connected to I_1 and I_2; O_3 is connected to $\text{NOT}(I_1)$ and I_2; and O_4 is connected to $\text{NOT}(I_1)$ and $\text{NOT}(I_2)$. Each NOT gate is represented by a triangle with a small circle at its output.	<pre>module decoder2x4 (input wire [1:0] in output reg [3:0] out); always @ (*) begin case (in) 2'b00: out = 4'b0001; 2'b01: out = 4'b0010; 2'b10: out = 4'b0100; 2'b11: out = 4'b1000; endcase end endmodule</pre>

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Notes on grading:

Both correct: Logic circuit + Verilog design = 1 + 1 points = 2 points in total;

A fully correct logic circuit – 1 point, any mistake (even minor) in logic circuit is penalized with (-1) point;

A fully correct Verilog HDL design – 1 point, otherwise Verilog errors are penalized as follows:

- No proper module declaration – (-0.5 points);

- Minor mistakes related to module declaration – (-0.2 points);

- Misuse of always, case, assign, if statements – (-0.4 points);

- Misuse of “begin/end” constructs – (-0.2 points);

- Misuse of logic gates declarations, missing declarations of wires and related – (-0.2 points);

- Other minor syntax mistakes – (-0.2 points)

- Misuse or lack of “reg” keyword, missing “;” in the line ends – not penalized

This is the end of the student book
Draft (will NOT be checked)